# OPERATOR'S ORGANIZATIONAL, DIRECT SUPPORT, GENERAL SUPPORT, AND DEPOT MAINTENANCE MANUAL INCLUDING REPAIR PARTS AND SPECIAL TOOLS LISTS <br> READER, PUNCHED TAPE RP-154(P)/G AND <br> TRANSMISSION IDENTIFICATION GENERATOR KIT MK-1583/G <br> (NSN 7440-00-997-8812) 

This copy is a reprint which includes current pages from Changes 1 through 8. Title was changed by Change 7 as shown above.

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## DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT

Be careful when working anywhere within the inclosure of this equipment. Serious injury or death may result from contact with high voltage terminals.

DON'T TAKE CHANCES!


# Operator's Organizational, Direct Support, General Support, and Depot Maintenance Manual for READER, PUNCHED TAPE RP-154(P)/G AND <br> TRANSMISSION IDENTIFICATION GENERATOR KIT MK-1583/G <br> (NSN 7040-00-997-8812) 

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11-85(1)
11-95(1)
11-98(1)
11-137(1)
11-302(1)
11-347(1)
11-367(1)
11-368(1)
11-500(AA-AC)(1)
29-134(1)
29-136(1)

NG: NONE
USAR: NONE
For explanations of abbreviations used see AR 310-50.

# Operator' s, Organizational, Direct Support, General Support, and Depot 

Maintenance Manual
for
READER, PUNCHED TAPE RP-154(P)/G
AND
TRANSMISSION IDENTIFICATION GENERATOR KIT MK-1583/G


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Figure 1-1. Reader, Punched Tape RP-154(P)/G, lee running spares.

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## CHAPTER 1

## INTRODUCTION

## Section I. GENERAL

## 1-1. Scope

This manual describes Reader, Punched Tape RP154(P)/G (punched tape reader) fig. 1-1), and contains operation and maintenance information. It also covers detailed functioning of the punched tape reader and includes the maintenance allocation chart app. C]. Refer to TM 11-7440-239-15/TO 31W4-4-11 NAVSHIPS 0967-324-0110 for installation and checkout procedures.

## 1-2. Indexes of Publications

a. DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.
b. DA Pam 310-7. Refer to DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

## 1-3. Forms and Records

a. Reports of Maintenance and Unsatisfactory Equipment. Maintenance forms, records, and reports which are to be used by maintenance personnel at all maintenance levels are listed in and prescribed by TM 38-750.
b. Report of Packaging and Handling Deficiencies. Fill out and forward DD Form 6 (Packaging Improvement Report) as prescribed in AR 700-8/NAVSUPINST 4030.29/AFR 71-13/MCO P4030.29A, and DSAR 4145.8.
c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 5538/NAVSUPINST 4610.33/AFM 75-18/ MCO P4610.19A, and DSAR 4500.15.

## 1-3.1. Reporting of Errors

The reporting of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submitted on DA Form 2028 (Recommended Changes to Publications and Blank Forms), and forwarded direct to Commander, US Army Electronics Command, ATTN: DRSEL-MA-Q, Fort Monmouth, NJ 07703 (Army); USAFLC Form 252 (Request for TO Revision or Change) and forward direct to prime ALC/MST \{Air Force); or forward to: Commander, Naval Electronics Systems Command, Code 4903, Washington, D.C. 20360 (Navy).

## 1-3.2. Reporting Equipment Improvement Recommendations (EIR)

EIR will be prepared using DA Form 2407, Maintenance Request. Instructions for preparing EIR's are provided in TM 38-750, The Army Maintenance Management System. EIR's should be mailed directly to Commander, US Army Electronics Command, ATTN: DRSEL-MA-Q, Fort Monmouth, NJ 07703. A reply will be furnished directly to you.

## 1-3.3. Administrative Storage.

For procedures, forms, and records, and inspections required during administrative storage of this equipment, refer to TM 740-90-1.

## 1-3.4. Destruction of Electronic Materiel

Demolition and destruction of electronic equipment will be under the direction of the commander and in accordance with TM 750-244-2.

## Section II. DESCRIPTION AND DATA

## 1-4. Purpose and Use

a. The punched tape reader (fig. 1-1) is used as a message input component of Digital Subscriber Terminal Equipment (DSTE) sets in the Automatic Digital Network (AUTODIN) military communications system. It reads messages prepared on paper tape by paper tape punch devices in eight-bit American Standard Code for Information Interchange (ASCII) or five-bit International Telegraphic Alphabet No. 2 (ITA-2).

It uses the perforated message tape to establish the information in electrical form and transmits the information in ASCII code to the common control unit (CCU) component of the DSTE set([fig. 1-2).
b. The punched tape reader is capable of reading eight-track, 1 -inch paper tape; and five-track 11/16-inch, $7 / 8$-inch, and 1 -inch paper tape in accordance with MIL.STD-188B. At high speed, the punched tape reader reads fully perforated paper tape and transfers data at a rate sufficient to maintain a line modulation rate up to and including 1,200 baud. At low speed the punched tape reader reads either fully perforated or chadless paper tape and transfers data at line modulation rates up to and including 150 baud.
c. The cabinet housing the punched tape reader is designed to contain one or two complete punched tape reader units each consisting of several assemblies. The option depends on whether one or two separate punched tape reader inputs to the CCU are required.

## Change 8 1-2



TM7440-219-15-2
Figure 1-2. Typical system application, block diagram.

## 1-5. Technical Characteristics of Punched Tape Reader

Input data
Paper tape perforated with either eight-bit ASCII or five-bit ITA-2 code and selected character printed on tape.
Output data $\qquad$ Eight-bit electrical data in ASCII form transferred on a bit-parallel, character-serial basis with the eighth bit maintaining odd parity.
Electrical interface $\qquad$ In accordance with MIL-STD-188B.
Tape sizes $\qquad$ Eight-track, 1 -inch paper tape, five track, 11/18., $7 / 8$., or 1 -inch paper tape.
Operating speed $\qquad$ Sufficient to maintain standard line modulation rates of 150, 300, 600, and 1,200 baud when connected to CCU
Power requirements $\qquad$ $120-$ volts $\mathrm{I}+12,-24$ ), $50 \mathrm{~Hz}(:$ : 2.5 ) or 60 Hz (:t3), single-phase, 4.3 amperes running current; 17 amperes starting current.

## 1-6. Items Comprising an Operable Equipment

a. Components.

b. Common Names. The following list provides the reference designation, official name, common name used in this manual, and the manufacturer's part number of each item listed. Although the full reference designations are shown below, abbreviated reference designations for subassemblies and subassembly components are frequently used in this manual.

| Reference designation | Item name | Common name |  | Mfg part No |
| :---: | :---: | :---: | :---: | :---: |
| A1, A4 | Logic assembly... | Logic assembly |  | A64752-001 |
| A1A1, A4A1 | PC card | Solenoid driver | ................ | A65209-001 |
| A1A3, A4A3 | PC card | Lamp driver |  | SM-E-546659 |
| A1A4, A4A4 | PC card | Interface control | (A65223-001 ${ }^{\text {r }}$ | A65215-001* |
| A1A5, A4A5 | PC card | Polar interface | (A65227-001or | A65205-001* |
| A1A6, A4A6 | PC card | Character decoder | ................. | A65421-001 |
| A1A7, A4A7 | PC card ............................... | Data register |  | A65425-001 |
| A1A8, A4A8 | PC card .............................. | ITA input code conv | verter........... | A53418-001 |


| Reference designation | Item name | Comm6n name | Mfg part No. |
| :---: | :---: | :---: | :---: |
| A1A9, A4A9 | PC card | Decode matrix. | A53725-001 |
| A1A10, A4A10 | PC card | Encode matrix .. | A53721-001 |
| A1A11, A4A11 | PC card ...... | Decode matrix ...................... | A53725-001 |
| AIA12, A4A12 | PC card ................................ | Encode matrix .............. | A53721-001 |
| A1A13, A4A13 | PC card | ASCII output code converter...... | A53434-001 |
| A1A14, A4A14 | PC card | Timing generator.. | A65433-001 |
| A1A15, A4A15 | PC card | Continuous step and alarm logic | A65437-001 |
| A1A16, A4A16 | PC card ..... | Control logic. | A65429-001 |
| A2, A5 | Reader mechanism assembly .... | Reader mechanism... | A64757-001 |
| A3, A6 | Control panel assembly.............. | Control panel.......................... | $\begin{aligned} & \text { A64758-001, } \\ & \text { A64758-002 } \end{aligned}$ |
| B1 | Blower . | Blower .... | SM-C-546250 |
| FL1 | Filter assembly ......................... | Filter ... | A64761-001 |
| PS1, PS2 | Power supply ........................... | Power supply.. | 810003-103 |
| PS1A1, PS2A1 | PC card | +4.75-volt regulator.. | 38864 |
| PS1A2, PS2A2 | PC card | +12-volt and-12-volt regulators | 38869 |
| PS1A3, PS2A3 | PC card | -48-volt regulator..................... | 38874 |
| PS1A12, PS2A12 | PC card | Sequence module ...................... | 38982 |

* The two PC cards listed are interchangeable.


## 1-7. Description of Punched Tape Reader

When ready for operation, the components of the punched tape reader are assembled as shown ir figure 1-1. The punched tape reader consists of one or two identical logic assemblies A1 and A4, one or two identical reader mechanisms A2 and A5, one or two identical control panels A3 and A6, one or two identical power supplies PS1 and PS2, a blower B1, and a filter assembly FL1. Since the two logic assemblies, reader mechanisms, control panels, and power supplies are identical, the following information covers the A1, A2, A3, and PS1 assemblies, but is also applicable to the A4, A5, A6, and PS2 assemblies, respectively.
a. Logic Assembly A1 (fig. 1-3), Logic assembly A1 contains a chassis which supports 15 printed circuit (PC) cards and the appropriate interconnection cabling required for the logic functions of the punched tape reader. Logic assembly A1 is slide-mounted in the inclosure. The slides and the handle on the front panel provide easy access to the chassis for maintenance.

## Change 6 1-3



Figure 1-3. Punched tape reader, showing location of major assemblies.
b. Reader Mechanisms fig. 1-3) Each of the reader mechanisms (A2 and A5) is a slide-mounted chassis consisting of a tape deck assembly, capstan drive mechanism assembly, read head and track assembly, network assembly, and amplifier assembly. The tape deck assembly, which contains the sensors and lamps, and the read head and track assembly protrudes from the front of the panel, while the capstan drive mechanism assembly, network assembly, amplifier assembly, drive motor, timing belts, and pulleys are mounted on the shelf at the rear of the panel. Two electrical connectors are located at the rear of the chassis for interconnection of each reader mechanism with its associated logic assembly and power supply (mounted directly below reader mechanism).
c. Control Panels (fig. 1-3). Each of the control panels (A3 and A6) consists of a panel containing pushbutton controls and indicators necessary for operation of the punched tape reader. Each control panel is mounted on the sloping surface of the inclosure below it's associated reader mechanism. This location provides for simultaneous viewing of the punched tape and the indicators on control panel.
d. Power Supply (fig. 1-3). Each of the power supplies (PS1 and PS2) is a slide-mounted chassis which supplies $+4.75,-12,+12$, and -48 volts dc, and 15 volts ac for operation of its associated paper tape reader.

Change 1-4

Each power supply is mounted directly below its associated logic assembly, and consist of a chassis containing all the regulated dc power supplies required for its associated tape reader. The front panel of each power supply chassis contains a separate fuse for each dc power supply, and fuses which protect the drive motor, the fan, and the indication lamps of the control panel. Spare fuses are also mounted on the front panel. The function and value of each fuse is marked in the front panel.
e. Blower B1 (fig. 1-3). Blower B1 is mounted behind the grill in the bottom of the inclosure. Blower B1 provides cooling air to the assemblies in the inclosure.
f. Filter Assembly FL1 fig. 1-3). Filter assembly FL1 is mounted at the left lower rear of the inclosure. Filter assembly FL1 filters the high frequency line noise from the ac power input to the power supplies.
g. Inclosure fig. 1-3). The inclosure is a freestanding cabinet that provides mounting surfaces for two logic assemblies, two reader mechanisms, two control panels, two power supplies, one blower, and one filter assembly. Access to the logic assemblies, power supplies, blower, and filter assembly is provided by two hinged doors at the front of the inclosure, and a hardware-mounted removable cover at the rear of the inclosure.

## Section III. DESCRIPTION AND DATA, TRANSMISSION IDENTIFICATION GENERATOR KIT, MK-1583/G

## 1-8. Purpose and Use

The transmission identification generator (TIG) is used on some punched tape readers to provide channel designation and channel sequence numbers in message transmission where traffic is introduced into the AUTODIN via DSTE, AN/FYA-71V. The TIG, when installed in the Punched Tape Reader RP-154(P)/G, is for use with the Common Control Unit (CCU) C-8120 (P)/G.

1-9. Technical Characteristics of the
Transmission Identification Generator Input data ----------------- Seven-bit electrical data in ASCII form transferred on a bit-parallel, character-serial basis from the punched tape reader.
Output data---------------- Eight-bit electrical data in ASCII form transferred on a bitparallel, character-serial basis with the eighth bit maintaining odd parity.
Operating speeds-------- Sufficient to maintain standard line modulation rates of 150, 300,600 , and 1,200 baud when connected to the CCU.

Power requirements -----15 VAC. + 4.75 VDC, + 12 VDC, and -12 VDC.

## 1-10. Components and Dimensions of Transmission Identification Generator Kit

a. Components. The TIG chassis is $31, / 2$ inches high, 17 inches wide, and 13 inches deep. Major components of the TIG kit are-

```
Quantity Item
    1 -----------------------Electrical chassis assembly
    1 ------------------------EM signal cable assembly
    1 ---------------------------- TIG to TIG cable assembly
    1 ------------------------Control logic PC card (punched
                        tape reader A1A2).
```

b. Common Names. The following list suppliments the list in paragraph 1-6 after the TIG kit has been installed in the punched tape reader. The list includes the reference designation, official name, common name used in this manual, and the manufacturer's part number of each item listed. Although the full reference designations are shown below, abbreviated reference designations for subassemblies and subassembly components are frequently used in this manual. Prefix the abbreviated reference designation with the applicable assembly or subassembly identification.

| Reference designation | Item name | Common name | Mfr part No. |
| :---: | :---: | :---: | :---: |
| A1A2, A4A2 ---------------- | PC card ------------------------------------ | Control logic ----------------------- | 12-890081 |
| A7, A8------------------------ | Transmission identification generator. | TIG assembly | 00-001501 |
| A7A1, A8A1 ----------------- | PC card ------------------------------------- | Counter logic ---------------------- | 12-890082 |

c. On-Site Parts Kit. A TIG on-sites repair parts kit, General Dynamics, Electronics Division, part number 05001283 (FSN 7440-042-8876), is available containing sufficient repair parts to provide a 12-month maintenance support of the TIG assembly.

## 1-11. Description of the Transmission Identification Generator

When ready for operation, the TIG assembly is secured to the top of the punched tape reader. Refer to figure 13. In single punched tape readers, the TIG is installed in the location designated $A 7$ which is on the top of the enclosure directly above the reader mechanism A2.

In dual punched tape readers, either one or two TIG kits may be installed. If the TIG assembly is to be used with the punched tape reader No. 1, it will be installed in the location designated A7 which is on the top of the inclosure directly above the reader mechanism A2. If it is to be used with punched tape reader No. 2, it will be installed in the location designated A8 which is on the top of the inclosure directly above the reader mechanism A5. The TIG kit consists of TIG assemblies A7 or A8, control logic PC card A1A2 or A4A2, EM signal cable assembly, TIG to TIG cable assembly, and mounting hardware. Since the two TIG assemblies A7 and A8 are identical, information in this manual refers to TIG assembly A7, logic assembly A1, and power supply PS1, but is also applicable to TIG assembly A8, logic assembly A4, and power supply PS2, respectively.
a. TIG Assembly A7 (iq. 1-4). The TIG assembly A7 consists of a chassis containing a control panel and a cable assembly providing TIG connection to the punched tape reader. The control panel contains the TIG controls and indicators and supports the counterl logic PC card A7-A1. The control panel is hinge-mounted for easy access to controls and PC card for maintenance.
b. Control Logic PC Card A1A2 [fig. 1-4]. The control logic assembly Al functions to inhibit normal paper tape reader operation during generation of a transmission identification sequence of ASCII coded alphabetical, numerical, and machine function characters at the start of each message.
c. EM Signal Cable Assembly. The EM signal cable is used to connect 15 VAC power from the power supply to the logic assembly and to connect the EM interface signal from the logic assembly to the interface plate.
d. TIG to TIG Cable Assembly. Although supplied in all TIG kits, the TIG to TIG cable assembly is used only in installations having both TIG assembly A7 and TIG assembly A8 installed. The cable functions to enable counters in both TIG assemblies to be simultaneously incremented regardless of which TIG,/punched tape reader is transmitting the message.


TM 7440-219-15-14
Figure 1-4. Transmission identification generator kit, showing major components.

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## CHAPTER 2

## OPERATING INSTRUCTIONS

## Section I. PUNCHED TAPE READER

## 2-1. Operator's Controls and Indicators

a. Control Panel Controls and Indicators fig. 2-1

| Control or Indicator | Function |
| :---: | :---: |
| AUDIBLE RESET | When pressed, discontinues audible |
| switch (Z1). | alarm at CCU which was sounding <br> to indicate punched tape reader |
| malfunction. |  |


| Control or indicator STOP switchIndicator (Z8). | Function |
| :---: | :---: |
|  | When pressed, stops operation |
|  | punched tape reader and causes |
|  | witch-indicator to light red. Also |
|  | lights red to indicate punched tape |
|  | reader is stopped by a cancel |
|  | signal from CCU or by detection of |
|  | ult condition (TIGHT TAPE, TAPE |
|  | , MOTION FAIL, or INVALID |
|  | CHARACTER indicator I |
| LOCAL TEST switch-indicator (Z9). | Operation of LOCAL TEST |
|  | switch-indicator lights in |
|  | amber and initiates local |
|  | processing of tape when punched |
|  | tape reader is not assigned and is |
|  | in stop mode. |
| DC POWER <br> indicator (DSI). | Lights white when all dc voltages are present in tape reader. |
| CANCEL indicator (DS2). | ghts red when cancel signal is |
|  | received from CCU. |
| INVALID CHARACTER indicator (DS3). | Lights red when character is |
|  | either invalid or is not contained in list of permissible characters. |
| MOTION FAIL indicator (DS4). | Lights red upon detection of tape motion failure. |
| TAPE OUT indicator (DS5). | After start-of-message signal is received, lights red when end of tape passes through tape reader before end-of-message function is received. |
| TIGHT TAPE indicator (DS6). | Lights red when tight tape condition is present. |
| NOT ASSIGNED | Lights amber when punched tape |
| indicator (DS7). | reader is not assigned at CCU. |



Figure 2-1. Control panel, controls and indicators.
b. Other Controls and Indicators.

Control or indicator Function
Code select switch Arranges punched tape reader
S1 (fig. 1-3. circuitry for operation with either ASCII or ITA 2 message tape.
RESET switch S2
fig. 1-3.
Slew lever (fig.
2-2).
Tape stops (fig.
2-2).

Used by maintenance personnel only.
Permits free movement of tape through the tape deck,
When in lower position, adjusts tape deck slot for 7/8-and 11/16

| Control or indicator | Function |
| :---: | :---: |
|  | in. wide tape; placed in upper |
| position for 1-in. wide tape. |  |
| Tight tape sensor | When pivoted counterclockwise, |
| [fig. 2-2]. | stops transmission automatically |
|  | until tight tape condition is cor- |
|  | rected. |

Power supply blown Light to indicate blown fuse. fuse indicators (fig. 2-3).

DRIVE MOT switch Permits turning off drive S1 (tit. 2-3)
motor without powering down unit. retaining TIG display number.


Figure 2-2. Reader mechanism controls.
Change 5 2-2


Figure 2-3. Power supply, front panel.

## 2-2. Types of Operation

a. The punched tape reader can be operated in either the on-line or local test mode of operation. Selection of the on-line mode of operation transfers control of the punched tape reader to the CCU. The local test mode is used for test and maintenance functions.
b. Perform the following sequence of procedures when operating the punched tape reader:
(1) Preliminary starting procedure (para 2-3).
(2) Loading procedure (para 2-4).
(3) Starting procedure (para 2-5).
(4) Operating procedure (para 2-6).
(5) Stopping procedure (para 2-7).

## 2-3. Preliminary Starting Procedure

a. Set the tape stop. (fig. 2-2) in the proper position for the width of tape to be used (up for $1-\mathrm{in}$. wide tape; down for $7 / 8$ or $11 / 16$-in wide tape).
b. Operate the code select switch(fig. 1-3) to ITA 2 for five-track tape or to ASCII for 8 -track message tape, as appropriate.
c. Press the AC POWER switch indicator on the control panel (fig. 2-1), Check to be sure that the AC POWER and DC POWER indicator are lighted.

## 2-4. Loading Procedure

a. Check the tape for correct headers and format.
b. While holding tape hold down cover assembly, press release button and allow spring-loaded hold down cover to move to open position. See caution below.

## CAUTION

When unloading tapes, always use the fingers to prevent excessively fast upward movement of tape hold down cover to avoid a sharp impact of cover against equipment panel. Failure to observe this precaution will result in a broken plastic hold down cover.
c. Thread tape through the tight tape sensor as shown in figure 2-2
d. Turn slew lever [fig. 2-2] to release wheel and sprocket gear assembly. Channel the tape across the tape deck. (Insure that sprocket feed holes are away from operator.) Be sure that the sprocket pins are aligned with the sprocket feed holes.
e. Press release button (fig 2-2), move tape hold down cover to closed position, then release button. See caution below.

## CAUTION

When closing the tape hold down cover, always press release button. Failure to observe this precaution will result in broken parts and premature wear and replacement of the carrier.
f. Manually move tape back and forth to insure that it is properly seated in the tape deck. This procedure also aligns star wheels and sprocket pins with the punched holes in the tape. Return slew lever(fig. 2-2) to the position that engages and locks the wheel and sprocket gear assembly. See caution below.

## CAUTION

During operation, the slew lever must always be in the locked position. If it is necessary to start the tape at a particular character, use the slew lever to release the assembly to permit manual movement of the tape to the desired character in the reader.
g. Press SINGLE FEED switch three or four times to advance the tape through the tape path.

Be sure the tape advances and that the MOTION FAIL indicator does not light.
h. Press the CANCEL switch on the common control unit (CCU) before transmitting a message. This clears any random characters that may be in the CCU logic and also checks the line between the digital subscriber terminal (DST) and the automatic digital message switching center (ADMSC).

## 2-5. Starting Procedures

a. Press the START switch-indicator on the control panel.
b. Check to see that the following indicator lamps are not lighted:
(1) STOP switch-indicator.
(2) All fault alarm indicators (TIGHT TAPE, TAPE OUT, MOTION FAIL, and INVALID CHARACTER indicators).

## 2-6. Operating Procedure

a. On-Line Mode. To read a message tape in the on-line mode, press the START switch-indicator; the START -switch-indicator should be lighted green. The tape is then read in response to select and step commands from the CCU. During tape reading, the START switch-indicator lights white.
b. Local Test Mode. To operate in the local test mode, the NOT ASSIGNED indicator and STOP switchindicator must be lighted. When these conditions exist, press the LOCAL TEST switch indicator and check to see that the STOP switch indicator lamp goes out and that the punched tape reader processes tape.

## 2-7. $\quad$ Stopping Procedure

a. Standby Condition. Normally, when the punched tape reader is not used for short periods of time during a work shift, the power is left on so that the drive motor runs continuously and the equipment, in effect, is in a standby condition. When in the on-line or local test mode, stop the punched tape reader by pressing the STOP switch-indicator.
b. Power-Down. To power-down the punched tape reader, press the STOP switch-indicator, then press the AC POWER switch-indicator.

## 2-8. Correcting Fault Condition

Whenever a fault condition occurs, the punched tape reader is automatically placed into the stop condition.

When this occurs, check, the control panel indicators to determine the cause of the fault. After taking appropriate action to correct the fault, press the START switchindicator to restore the punched tape reader to the online condition.

## 2-9. Operation Checkout Procedure

To insure that the punched tape reader is providing correct output copy, operate it with the CCU as described in TM 11-7440-238-15.

## Section II. TRANSMISSION IDENTIFICATION GENERATOR

## 2-10. Operator's Controls and Indicators

a. Control Panel Controls and Indicators(fig. 2-4).

Control or indicator
ON-LINE /OFF-LINE switch(S1).

MANUAL
SEQUENCE NUMBER switch (S2).
LOAD switch(S3)

TIG ON indicator (DS1)
NEXT NUMBER indicator (DS2).

## Function

ON-LINE position enables TIG assembly A7 or A8 to generate a 13 to 16 character TI sequence at the beginning of each message. OFF-LINE position enables punched tape reader to function in a normal manner.
UPDATE Three section, 10 position each, switch used to select a count to be manually loaded into the channel sequence counter. Operates in conjunction with LOAD switch S3.
When momentarily depressed causes the count set into the MANUAL UPDATE SEQUENCE NUMBER switch S 2 to be loaded into channel sequence counter. This switch is inoperative if the punched tape reader START switch indicator $\mathrm{Z7}$ is illuminated white.
Lights white when the ON-LINE,/OFF-LINE switch (S1) is in the ON-LINE position.
Three section visual display of the channel sequence number to be transmitted as a part of the TI sequence of the next message. Power-up of the punched tape reader will clear the display to 000. Display counter can be manually loaded to any number from 000 through 999 by using the MANUAL UPDATE SEQUENCE NUMBER switch (S2) and the LOAD switch (S3).


Figure 2-4. TIG control panel, controls and indicators.

## 2-11. Types of Operation

a. The punched tape reader with TIG installed can be operated in either the on-line or local test mode of operation. Selection of the on-line mode of operation transfers control of the punched tape readel to the CCU. When the punched tape reader is in on-line mode, it can also operate with the TIG assembly in either the on-line or off-line mode. When the TIG is in the off-line mode, the punched tape reader will function in the same manner as described in section llabove.

If the TIG is placed in the on-line mode, the 13 to 16 character transmission identification sequence will be transmitted at the beginning of each message. The punched tape reader local test mode is used for test and maintenance functions. The TIG is inoperative when the punched tape reader is in the local test mode.
b. Perform the following sequence of procedures when operating the punched tape reader with TIG installed:
(1) Preliminary starting procedure (para 2-12).
(2) Punched tape reader operation (para 2-13).

## 2-12. Preliminary Starting Procedure

a. Perform the preliminary starting procedures outlined for the punched tape reader in paragraph 2-3.
b. After pressing the AC POWER switch indicator on the punched tape reader control panel, check to be sure the TIG control panel NEXT NUMBER indicators read "000."
c. Determine mode of TIG operation.
(1) TIG off-line mode. Place the TIG ON-LINE, OFF-LINE switch in the OFF-LINE position. Check to be sure the TIG ON indicator is not lighted and then operate punched tape reader following procedures outlined in baragraphs 2-4 through 2-9
(2) TIG on-line mode. Place the TIG ON-LINE OFF-LINE switch in the ON-LINE position. Check to be sure the TIG ON indicator is lighted white. If the next channel sequence number is to be other than 000, set the MANUAL UPDATE SEQUENCE NUMBER thumbwheel switch desired message number and press the LOAD switch. Check to be sure the NEXT NUMBER displays the proper count.

## NOTE

If operating at a terminal with two TIG assemblies that are both in the online mode, it is necessary to load the same channel sequence number into both TIG assemblies.

## 2-13. Punched Tape Reader Operation

Operate the punched tape reader in the normal manner following procedures outlined in paragraphs 2-4 through 2-9. In addition, observe that the NEXT NUMBER indicator count increments by one at the start of each message.

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## CHAPTER 3

## FUNCTIONING OF PUNCHED TAPE READER

## Section I. GENERAL FUNCTIONING

## 3-1. Punched Tape Reader, Block Diagram

 (fig. 3-1)All of the tape handling and reading functions of the punched tape reader are performed by the reader mechanism. With this mechanism, the message tape is advanced one character at a time and the punched holes are read.

Processing of the data read from the tape and control of the tape advance are performed by electronic circuits in the logic assembly and by manual switches on the control panel. These functions are described in baragraphs 3-2 through 3-8

## 3-2. $\quad$ Read Cycle

The tape is advanced by one character each time a new character is to be read. The advance command is given to the reader mechanism in the form of a solenoid advance pulse. This pulse is produced by a timing generator which goes through a timing sequence called a read cycle each time the tape is to be advanced. The solenoid advance pulse is produced at the beginning of each read cycle. The data read from the character which is advancing in the reading position is then evaluated at a later point in the read cycle. Read cycles may be initiated under remote control or under local control.

## 3-3. Remote Control of Read Cycle

When the punched tape reader is operated with the Common Control Unit (CCU), the tape is advanced in response to a step/data acknowledge pulse from the CCU whenever the CCU is prepared to receive a new character.
a. Automatic tape feed under control of the CCU is accomplished by operation of an appropriate start switch on the control panel. This supplies a ready signal to the CCU and enables advance control circuits in the logic assembly to operate under CCU control.
b. Upon receipt of a ready signal from the punched tape reader (fig. 3-2), the CCU operator must assign the punched tape reader to operate with the CCU, by operating a front panel switch on the CCU. This action results in an assigned signal which is routed from the CCU through receive interface circuits to the advance control circuits in the logic assembly of the punched tape reader. This permits the CCU to select the punched tape reader for a message by sending a select signal and a step/data acknowledge pulse. These signals enable the advance control circuits to begin tape advance operations.

Note. Most signals shown in figure 3-2 are high when active. This is the format used in the punched tape reader. Conversion by the receiver and transmit interface circuits causes most of the actual received and transmitted control signals to be inverse (low when active) on the signal lines connecting the CCU and punched tape reader.
c. Initially, when the start switch on the control panel is operated, the tape advances to the beginning of a message. This is controlled automatically by the advance control circuits which begin operation in a mode called the remote continuous step mode.

In this mode, the ready signal to the CCU is disabled. Thus, the CCU cannot begin controlling tape advance until the punched tape reader has stepped through the leader tape.
d. The advance control circuits generate an advance signal which allows the timing generator to go through repeated read cycles as long as the punched tape reader remains in the remote continuous step mode. At the beginning of each read cycle, a solenoid advance pulse is generated which causes the tape to be advanced to a new character position by momentarily energizing a solenoid in reader mechanism.
e. It is necessary to check the idle characters (space, blank, line feed, carriage return, etc) in the leader portion of the tape since the first non-idle character indicates the start of the message. Sensing switches in the reader mechanism read out the punched hole pattern in the form of logic signals. The hole pattern consists of eight bits when the tape is coded in ASCII and five bits when the tape is coded in ITA-2. In either case, the signals are generated on parallel lines and stored in a data register. Each character is stored under control of an input data sample pulse which is produced at a point in the read cycle when the switch contacts are sensing the hole pattern. This is based on the fact that a fixed time delay exists between the time the solenoid advance pulse is received by reader mechanism and when the new character is in position to be read.
$f$. The data remains stored in the input register from the beginning of the data sample pulse until the beginning of the next read cycle. During this time, the data is checked for invalid characters and transmitted to the CCU. If an ASCII tape is used, the data is routed through data select gates to a character decoder which decodes the data and monitors for idle or invalid characters. If an ITA-2 is used, the data must be converted to ASCII before it can be decoded by the character decoder. This function is performed by an ITA2 to ASCII converter. The ASCII data is then routed through the data select gates to the character decoder. Selection between ITA-2 and ASCII operation is controlled by code select switch S1 on the maintenance panel of logic assembly.
g. As long as idle characters are read from the tape, the character decoder supplies an idle character signal to the advance control circuits. This permits continued advance of the tape.

When the first non-idle character is detected, the advance control circuits are switched out of the remote continuous step mode and into the ready mode. In this mode, the ready line to the CCU is activated.
$h$. When the CCU is ready to accept the message, the select and step/data acknowledge lines to the punched tape reader are activated, which permits the advance control circuits to cause the generation of one read cycle. The data stored in the input data register is now made available through the data select gates (and, if necessary, the ITA-2 to ASCII converter) for transmission to the CCU through the transmit interface circuits. No significant delays occur in any of the circuits between the input data register and the CCU.
i. To insure evaluation of the data bit lines by the CCU at the proper time, the timing generator sends out a data strobe pulse through the transmit interface circuits to the CCU. The data strobe pulse is generated after the data has been stored in the input data register.
$j$. The data strobe pulse allows the CCU to read the contents of the data bit lines and also causes the CCU to deactivate the step/data acknowledge line, to prevent another read cycle from being initiated until the CCU has had the opportunity to evaluate the character.

When evaluation is complete, the step/data acknowledge line is again activated and another read cycle is initiated.
$k$. The read cycle process continues until 80 characters have been transmitted to the CCU. The CCU processes data in 80 -character blocks. Thus, the delay in activating the step/data acknowledge line after the 80th character is somewhat longer than after the other characters. The CCU marks the end of the block by transmitting an end of block (EOB) signal to the tape reader. This signal extends from the 80th character data strobe to the first character data strobe of the next block. An additional signal with the same timing is supplied by the CCU following the end of message sequence in the last block in a message. This signal is called the end of message (EOM) signal.
I. Both the EOB and EOM signals are routed through the receive interface circuits. When these signals are received simultaneously, the advance control circuits consider the message completed and reactivate the remote continuous step mode. This action allows the tape to be automatically stepped through the idle characters between messages until the first non-idle character of the next message is detected or the end of tape is reached.

Change 2 3-4
 by interface receive and transmit circuits.

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Figure 3-2. Punched tape reader, timing diagram.

## 3-4. Local Control of Read Cycle

When the assigned line from the CCU is inactive, the operator can initiate read cycles manually by operation of appropriate switches on the control panel. Continuous read cycles are enabled when the local test mode is selected. Single read cycles can be initiated by each operation of a SINGLE FEED switch.

## 3-5. Alarm Functions

Various operations of the punched tape reader are continuously checked by a group of alarm circuits in the logic assembly.
a. Alarm Stop. When the critical alarm condition occurs, an alarm stop signal is generated which disables the advance control circuits, thereby interrupting the ready signal to the CCU.

The alarm stop signal is also supplied directly through the transmit interface circuits to the CCU, which causes an audible alarm at the CCU to be activated. The following fault conditions can cause an alarm stop:
(1) Invalid character. An invalid character read from the tape is a sign of a defective tape or defective punched tape reader circuits. This condition is indicated by the character decoder which monitors the ASCII data bit output lines for invalid character codes.
(2) Tape. motion. Since the evaluation of data read from the tape by the punched tape reader depends on proper tape motion, spurious character readouts may occur if the tape fails to advance.

The tape advance is sensed by a tape motion sensor in the reader mechanism. If the tape fails to advance or advances too slowly, a corresponding tape alarm signal is produced to activate the alarm circuits in the logic assembly.
(3) Tape-out. A tape-out condition caused by the end of the tape or a break in the tape is sensed by a tape out sensor switch in the reader mechanism. When a tape out condition occurs during a message, a corresponding tape alarm signal is produced.
(a) A special case arises if a special header (a two-tape) message is being read by the punched tape reader. When the tape out condition occurs at the end of the header tape, it is undesirable to transmit an alarm stop signal to the CCU, since no alarm condition exists and the message is still in progress.
(b) To prevent this, a special pilot header switch is used as the control switch to start operation for the header tape. This action allows normal read cycle control by the CCU, but causes a pilot header signal to be produced which disables the tape-out alarm stop function.
(c) At the end of the header tape, the tape-out signal activates an operator's stop command to the advance control circuits. Thus, read cycles are stopped and the ready line to the CCU is deactivated. The CCU must now wait for the punched tape reader to be ready again before transmitting another step/data acknowledge pulse. When the second message tape is loaded, the tape reader operator initiates tape feed operation in the normal manner, thereby restoring the ready signal to the CCU.
(4) Cancel. An alarm stop signal is generated whenever a cancel signal is received from the CCU. This signal, routed through the receive interface circuits, is generated when the CCU discovers a parity error in the data or when the CCU receives a reject message (RM) instruction from the switching network to which the data is routed by the CCU.

The CCU operator may also initiate a cancel manually by operation of a front panel switch.
b. Operator Alarm. When a tight tape condition is sensed in the reader mechanism, the resulting tape alarm signal to the alarm circuits causes an operator alarm signal to be generated. This signal is routed through the transmit interface circuits to the CCU and is also fed back to the advance control circuits to disable tape advance and to interrupt the ready signal to the CCU.
c. Audible Alarm Reset. When the audible alarm is sounded in the CCU as a result of a punched tape reader alarm condition, this alarm can be reset by operating the Audible Reset switch on the panel. Operation of this switch results in transmission of an audible alarm reset signal through the transmit interface circuits to the CCU.

## 3-6. $\quad$ Signaling Code

a. The signaling code used by the punched tape reader to transmit data to the CCU is the eight-bit ASCII code shown in the signaling code chart (fig. 3-3). Seven of the ASCII bits contain the data. The eighth is a parity bit which is added or left out, as necessary, to have odd parity for each character.
$b$. The data on the message tape may be in the five-bit ITA-2 code or the eight-bit ASCII code. The ITA-2 code for each character is shown ir figure 3-3. Seven of the characters which can be read by the punched tape reader are idle characters which may be used for leader tape. These are identified by an asterisk irffigure 3-3.

NOTE: ASCII code signals transmitted from the punched tape reader to the CCU are ODD parity as shown in figure 3-3. ASCII code signals read from the punched tape are EVEN parity (column 8 (parity signal) opposite to those shown in figure 3-3).

| CHARACTER |  | ASCII punched code 8 (P) 7654321 (columns) |  | ITA-2 <br> punched code <br> 54321 <br> (columns) |
| :---: | :---: | :---: | :---: | :---: |
| Symbol | Name |  |  |  |
| - | Hyphen | 1 | 0101101 | 00011 |
| . | Period | 1 | 0101110 | 11100 |
| 1 | Slant | 0 | 0101111 | 11101 |
| $\emptyset$ | Zero | 1 | 0110000 | 10110 |
| 1 | One | 0 | 0110001 | 10111 |
| 2 | Two | 0 | 0110010 | 10011 |
| 3 | Three | 1 | 0110011 | 00001 |
| 4 | Four | 0 | 0110100 | 01010 |
| 5 | Five | 1 | 0110101 | 10000 |
| 6 | Six | 1 | 0110110 | 10101 |
| 7 | Seven | 0 | 0110111 | 00111 |
| 8 | Eight | 0 | 0111000 | 00110 |
| 9 | Nine | 1 | 0111001 | 11000 |
| : | Colon | 1 | 0111010 | 01110 |
| ; | Semicolon | 0 | 0111011 | 11110 |
| < | Less than | 1 | 0111100 |  |
| = | Equals | 0 | 0111101 |  |
| > | Greater than | 0 | 0111110 |  |
| ? | Question mark | 1 | 0111111 | 11001 |
| $\backslash$ | Grave accent | 0 | 1000000 |  |
| A | A | 1 | 1000001 | 00011 |
| B | B | 1 | 1000010 | 11001 |
|  |  |  | TM 74.4 | 15-8 (2) |

Figure 3-3(1). Signaling code chart (part 1 of 4).

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| CHARACTER |  | ASCII punched code <br> 8 (P) 7654321 (columns) |  | ITA-2 <br> punched code 54321 (columns) |
| :---: | :---: | :---: | :---: | :---: |
| Symbol | Name |  |  |  |
| *NUL | Null (blank) | 1 | 0000 000 | 00000 |
| BEL | Bell | 0 | 0000111 | 00101 |
| *LF | Line feed | 1 | 0001010 | 00010 |
| * CR | Carriage return | 0 | 0001101 | 01000 |
| *SO | Shift out (figures) | 0 | 0001110 | 11011 |
| *SI | Shift in (letters) | 1 | 0001111 | 11111 |
| *SP | Space | 0 | 0100000 | 00100 |
| DC4 |  | 1 | 0010010 |  |
| ! | Exclamation point | 1 | 0100001 | 01101 |
| EM |  | 0 | 0011001 |  |
| " | Quotation mark | 1 | 0100010 | 10001 |
| \# | Number sign | 0 | 0100011 | 10100 |
| \$ | Dollar sign | 1 | 0100100 | 01001 |
| \% | Percent sign | 0 | 0100101 |  |
| \& | Ampersand | 0 | 0100110 | 11010 |
| , | Apostrophe | 1 | 0100111 | 01011 |
| $($ | Opening parenthesis | 1 | 0101000 | 01111 |
| ) | Closing parenthesis | 0 | 0101001 | 10010 |
| * | Asterisk | 0 | 0101010 |  |
| + | Plus | 1 | 0101011 |  |
| , | Comma | 0 | 0101100 | 01100 |
| TM 7440-219-15-8 (1) |  |  |  |  |

Figure 3-3(2). Signaling code chart (part 2 of 4).

Change 2 3-8

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| CHARACTER |  | ASCII punched code 8(P) 7654321 (columns) |  | ITA-2 <br> punched code <br> 54321 <br> (columns) |
| :---: | :---: | :---: | :---: | :---: |
| Symbol | Name |  |  |  |
| C | C | 0 | 1000011 | 01110 |
| D | D | 1 | 1000100 | 01001 |
| E | E | 0 | 1000101 | 00001 |
| F | F | 0 | 1000110 | 01101 |
| G | G | 1 | 1000111 | 11010 |
| H | H | 1 | 1001000 | 10100 |
| I | 1 | 0 | 1001001 | 00110 |
| J | J | 0 | 1001010 | 01011 |
| K | K | 1 | 1001011 | 01111 |
| L | L | 0 | 1001100 | 10010 |
| M | M |  | 1001101 | 11100 |
| N | N | 1 | 1001110 | 01100 |
| O | 0 | 0 | 1001111 | 11000 |
| P | P | 1 | 1010000 | 10110 |
| Q | Q | 0 | 1010001 | 10111 |
| R | R | 0 | 1010010 | 01010 |
| S | S | 1 | 1010011 | 00101 |
| T | T | 0 | 1010100 | 10000 |
| U | U | 1 | 1010101 | 00111 |
| V | V | 1 | 1010110 | 11110 |
| w | W | 0 | 1010111 | 10011 |
|  |  |  |  | TM 7440-219 15-8 (3) |

Figure 3-3. Signaling code chart (part 3 of 4).
Change 2 3-9

| CHARACTER |  | ASCII punched code 8(P) 7654321 (columns) |  | ITA-2punched code54321(columns) |
| :---: | :---: | :---: | :---: | :---: |
| Symbol | Name |  |  |  |
| X | X | 0 | 1011000 | 11101 |
| Y | Y | 1 | 1011001 | 10101 |
| Z | Z | 1 | 1011010 | 10001 |
| [ | Opening bracket | 0 | 1011011 |  |
| $\sim$ | Tilde | 1 | 1011100 |  |
| $\wedge$ | Circumflex | 0 | 1011110 |  |
| - | Underline | 1 | 1011111 |  |
| @ | Commercial at | 1 | 1100000 |  |
| *DEL | Delete | 0 | 1111111 |  |

TM 7440-219-15-8 (4)

## Figure 3-3(4) Signaling code chart (part 4 of 4).

## Section II. MECHANICAL FUNCTIONING

## 3-7. General

The mechanical portion of the punched tape reader consists of a reader mechanism assembly A2 which is covered in the following paragraphs.

## 3-8. Reader Mechanism Assembly A2, Block Diagram (fiq. 3-4)

a. The reader mechanism receives prepunched paper tape which is fed to the tape deck and read head and track assembly, where the information in the tape is sensed, and transmitted to the logic circuitry.
b. The operation begins with a solenoid drive pulse from the logic section being applied to the electromagnet on the forward escapement assembly. A clutch within the mechanism assembly, operating in response to the step command signal, allows the drive motor to turn the capstan through a gearing arrangement within the mechanism assembly, The capstan, which is essentially a
toothed wheel, engages the sprocket holes of the punched tape, and advances the tape through the tape deck, one character for each drive pulse.
c. Electrical contacts within the read head and track assembly sense the presence or absence of data holes in the punched tape, through eight read switches (one per tape track). The condition of each switch becomes the bit output data information which is transmitted to the logic circuitry through an electrical connector.
d. The punched tape reader incorporates several sensing devices to provide signals to the logic circuitry if malfunctions occur. These devices consist of an end of tape switch, a tight tape sensor, and a tape motion sensor. The tight tape sensor provides an indication to the logic circuitry if an obstruction occurs which prevents the punched tape from advancing. The end of tape switch provides an indication to the logic circuitry four to six characters before the end of the tape. The tape motion sensor provides a continuous indication to the logic circuitry (through a
photocell and amplifier circuit) where the timing is checked to make sure that the tape is advancing properly in response to commands. The three alarm circuit outputs provide panel lamp indications any of the three malfunctions occur.
e. A slew lever on the front panel disengages the mechanism and allows the tape to be manually slewed through the read head for proper positioning. When the tape is positioned as desired, releasing the slew lever indexes the tape for the next reading command.


Figure 3-4. Reader mechanism assembly, block diagram.

## 3-9. Capstan Drive Mechanism Assembly

## [fig. 3-5)

Power is applied from the motor drive pulley through a belt to the driven pulley which turns a shaft and gear assembly. A bevel gear transfers the power to a friction clutch through a clutch drive gear. When no step command signal is received. the escapement coil armature is engaged
with the friction clutch, causing the clutch to slip, and the capstan is stationary. When the solenoid drive pulse energizes the escapement coil, the armature releases the friction clutch momentarily, and the capstan rotates one step (character) forward. The armature latches against the next tooth of the friction clutch, stopping the motion until the next drive pulse.


Figure 3-5. Capstan drive mechanism assembly.

## 3-10. Read Head and Track Assembly

## fig. 3-6)

The read head and track assembly consists of eight identical sets of read switches, one for each data track on the punched tape. The read switches sense the presence or absence of holes in the
tape in the following manner: When a hole (perforation) in the tape moves into position as the punched tape rides along the capstan, one of the four points in the starwheel rises through the hole. Since the starwheel lever is free to pivot about a pin, pressure from a movable wire con-
tact causes the contact to switch to the upper fixed contact position. An electrical pulse sent through the movable wire contact to the upper fixed contact provides the output indication to the logic circuitry for this condition. In the same way, when a no-hole condition in the tape is in position, the starwheel does not go through the tape, and the pressure exerted causes the movable wire contact to switch to the lower fixed contact.

## 3-11. Tape Deck Assembly

(fig. 3-7)
The tape deck assembly contains the end of tape switch, tape motion sensor, tape holddown assembly, and tape guides to maintain the punched tape in the proper position.


Figure 3-6. Read head and track assembly.

TAPE HOLD DOWN
ASSEMBLY


Figure 3-7. Tape deck assembly.

## 3-12. End of Tape Switch

(fig. 3-8)
The end of tape switch provides a switch contact transfer to indicate the end of the punched tape. Both the normally open and normally closed con-
tacts are electrically connected so that an indication is always present. In the unactuated position as shown in figure $3-8$, the actuator protrudes through the tape path. When the tape passes over the sensing area, the actuator pivots about a pin
and closes the switch contact. Only two contacts of the switch are used. When tape is in read head, the switch is open. When no tape is in read head, the switch is closed.


Figure 3-8. End of tape switch.


3-13. Tape Motion Sensor
fig. 3-9
The tape motion sensor consists of a light source (part of lamp mounting card assembly), a photo-cell (part of light sensor mounting card assembly), and a tape-driven capstan (with shutter holes), rotating between them, all mounted in a housing under the left side of the tape deck assembly. As the tape rotates the capstan, the shutter holes act as a focal plane shutter between the light source and the photocell to provide a dark-light-dark sequential input for each character step of the tape. The sensor output pulse is shaped and amplified by the amplifier assembly (fig. 34), and then sent to the logic circuitry for timing comparisons.


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Figure 3-9. Tape motion sensor(

## 3-14. Tight Tape Sensor

fig. 3-10
The tight tape sensor consists of rollers, a cam, a switch, and an actuator, designed to close the switch if a malfunction occurs that involves a jam caused by tangled tape or other conditions which stop the tape at the sensor. During normal operation, the roller support is in the position shown as the tape feeds to the tape deck. The switch is unactuated, and the logic circuits
establish a +4.5 -volt level at the normally open switch terminal. In a tight tape condition, the capstan pulls the tape, which now resists the pull, and the roller support, which pivots about a shaft on the center of the large roller, rotates counterclockwise. This rotation causes the cam, which is mounted on the same shaft as the large roller, to turn so that the larger diameter of the cam moves the actuator forward, closing the switch and providing a ground output at the normally open contact.


Figure 3-10. Tight tape sensor.

## Section III. ELECTRICAL FUNCTIONING

## 3-15. Logic Diagrams

a. Most of the data processing and control functions of the punched tape reader are performed by logic circuits on the printed circuit cards in logic assembly AI. Thus, the electrical operation of each PC card is represented in chapter 8 by a logic diagram rather than a conventional schematic diagram. The logic diagram shows all input and output connections of the PC card including power connections but does not show the circuit components which make up the individual logic elements.
b. Most of the logic elements in the punched tape reader are mounted in integrated circuit modules. Thus, detailed circuit components are not applicable. (Each integrated circuit logic element is considered to be a single electrical component.) For those logic elements that are made up of discrete circuit components, the schematic representation and a description of the circuit operation for each type of logic element are given in baragraphs 3-7d through 3-73.

Note. For convenience, all PC cards in logic assembly Al are identified only by their distinguishing reference designations (AI, A2, A3, etc.). These designations should be prefixed by Al to form the complete designation.

## 3-16. Logic Signal Notation

a. In general, logic signals in the punched tape reader switch between a high level of +4.5 volts and a low level of 0 volt. Some signal lines are considered activated when the level is high while others are considered activated when the level is low. The state indicators (small circles) at the input and output of logic elements indicate which lines are activated by a high level (state indicator absent) and which lines are activated by a low level (state indicator present).
b. All significant logic signals are assigned a functional name or designation. To permit the active state of a signal to be indicated by its functional name, the high level is arbitrarily designated true or logical for signal naming purposes and the low level is arbitrarily designated false
or logic 0 . Thus, the signal is a true-function if it is active on a high level and a not-function if it is active on a low level. Not-function signal names are prefixed by the letter N (for example: NASG: not assigned).
c. In the functional descriptions, the terms high and low are used for +4.5 -volt and 0 -volt levels. Pulses or steps going from 0 volt to +4.5 volts are called positive pulses or steps and those going from +4.5 volts to 0 volt are called negative pulses or steps.

## 3-17. Logic Diagram Symbol Notation

a. Typical integrated circuits and discrete circuit logic elements are shown in figure \&-10. Inputs and outputs of integrated circuit logic elements are identified by the wire terminal numbers of the integrated circuit modules in which the elements are located.
b. Three tagging lines are used within each logic symbol for identification purposes.
(1) The first tagging line in each symbol identifies the logic element type. The various types of integrated circuits and discrete circuit logic elements are described in paragraphs 3-18 through 3-22
(2) The second tagging line in each logic symbol identifies the reference designation of the logic element. This reference designation must be preceded by the PC card reference designation to form the complete designation of the logic element.

## 3-18. Integrated Circuit Modules

a. The integrated circuit modules used in the punched tape reader are of several types as described in the following subparagraphs. However, all are of standard construction and wired to the printed circuit cards through 10 terminals ( 1 through 10). Reference designations for the integrated circuit modules are Z 1 , Z2, Z3, etc.
b. Some of the integrated circuit modules contain only one logic element while others contain two. Where two logic elements are contained in one integrated circuit module, the two elements are shown separately on the logic diagrams and are designated A and B (for example: Z1A and Z1B). The output signal terminal of the A element in each integrated circuit module is always terminal 2 and the output signal terminal of the $B$ element is always terminal 10.
c. Power supply inputs to the individual logic elements are not shown on the logic diagrams because there is no provision for them in logic symbology. However, all integrated circuit modules receive power supply inputs of 44.5 volts at terminal 6 , and ground at terminal 1.
d. Since the integrated circuits are of a standard construction, not all inputs to AND gates and OR gates are used in each application. Unused gating inputs are always wired to one of the used gating inputs. Thus, more than one terminal may be listed at an input on the logic diagram symbol.
e. Most integrated circuit logic elements can 8 function in more than one way. Thus, every AND gate for high inputs is an OR gate for low inputs and every OR gate for low inputs is an AND gate for high inputs. A noninverting OR gate becomes a simple buffer if the inputs are wired together and an inverting OR gate becomes an inverter if the inputs are wired together.
f. The logic operation of each integrated circuit module type is described in paragraph 3-19

## 3-19. Operation of Individual Integrated Circuit Modules

The operation of the individual integrated circuit modules used in the punched tape reader is described below. Logic symbols are given for each type of module, using typical tagging lines.
a. Type A-1 Module. Two type A-1 gates are located on each type A-1 module (fig. 3-11). These gates may be noninverting AND gates for high inputs (case A) or noninverting OR gates for low inputs (case B). Open circuit inputs are equivalent to high levels.
b. Type A-2 Module. One type A-2 gate is located on each type A-2 module (fig. 3-12). This gate may be a noninverting AND gate for high inputs (case A) or a noninverting OR gate for low inputs (case B). Open circuit inputs are equivalent to high levels. Terminal 10 is not used on type A2 modules.
c. Type E-i Module. Two type E-1 gates are located on each type E-1 module (tig. 3-13), These gates may be noninverting OR gates for high inputs (case A) or noninverting AND gates for low inputs. The type E-1 gate outputs are used only as expander inputs for $\mathrm{N}-3$ and $0-3$ modules ( f and h , below). Open circuit inputs to type El gates are equivalent to low levels.

PAPER TAPE READER LOGIC SIGNALS-MNEMONICS AND FUNCTIONAL NAMES

| AAR | AUDIBLE ALARM RESET | PRST | - | POWER ON RESET |
| :---: | :---: | :---: | :---: | :---: |
| ASG | ASSIGNED | RDY | - | READY |
| AS - | ADVANCE SOLENOID | RST | - | RESET |
| NASD | ADVANCE SOLENOID DRIVE | RRST | - | REGISTER RESET |
| AM - | ALARM | RSTO | - | RESET NORMALLY OPEN |
| AR - | ALARM RESET | RCS | - | REMOTE CONTINUOUS STEP |
| ARO | AUDIBLE RESET OPEN | RCSR | - | REMOTE CONTINUOUS STEP |
| ARC | AUDIBLE RESET CLOSED |  |  | RESET |
| ASW | ASC II SWITCH | RASD | - | RESET ADVANCE SOLENOID |
| BEL | BELL |  |  | DRIVE |
| CR - | CARRIAGE RETURN | STPO | - | STOP NORMALLY OPEN |
| CB - | - CLOSE BRACKET | SF | - | SINGLE FEED |
| CSTP | CONTINUOUS STEP TEST POINT | SFO | - | SINGLE FEED OPEN |
| CC - | CYCLE COMPLETE | SFC | - | SINGLE FEED CLOSED |
| CYCL | CYCLE | STC | - | START CLOSED |
| CRST | COUNTER RESET | STO | - | START OPEN |
| DST | DATA STROBE | SASD | - | SET ADVANCE SOL.. DRIVE |
| DTMF | DISPLAY TAPE MOTION FAILURE | STP | - | STOP |
| DCAN | DISPLAY CANCEL | SOS | - | SET OPERATOR STOP |
| DTO | DISPLAY TAPE OUT | SO | - | SHIFT OUT |
| DINC | DISPLAY INVALID CHARACTER | SI |  | SHIFT IN |
| DTT | DISPLAY TIGHT TAPE | SP | - | SPACE |
| DINH | DATA INHIBIT | SEL | - | SELECT |
| DSW | DISPLAY START WHITE | SDA | - | STEP DATA ACKNOWLEDGE |
| DSG | DISPLAY START GREEN | SINH | - | STEP INHIBIT |
| DEL | DELETE | TDST | - | TRANSMIT DATA STROBE |
| EOM | END OF MESSAGE | TT | - | TIGHT TAPE |
| EOB | END OF BLOCK | TMS | - | TAPE MOTION SET |
| GS - | GATED STEP | TM | - | TAPE MOTION |
| HSI- | HIGH SPEED INHIBIT | ALS | - | ALARM STOP |
| HSC | - HIGH SPEED COUNT | ARC | - | AUDIBLE RESET (NC) |
| IDC- | IDLE CHARACTER | ARO | - | AUDIBLE RESET (NO) |
| INC- | INVALID CHARACTER | BS | - | BACKSPACE |
| ISW | - ITA SWITCH | CAN | - | CANCEL |
| IDS- | INPUT DATA STROBE | CCAN | - | CCU CANCEL |
| INH- | INHIBIT | CDB1 | - | CCU DATA BIT 1 (2, etc through 8) |
| LF - | LINE FEED | CDC | - | CCU DATA CONTROL |
| LTR | LETTERS | CDS | - | CCU DATA STROBE |
| LSI - | LOW SPEED INHIBIT | CLK1 | - | CLOCK 1 |
| LTO | LOCAL TEST OPEN | CLXK | - | CLOCK 2 |
| LTC | LOCAL TEST CLOSED | CNA | - | CCU NOT ASSIGNED |
| LT - | LOCAL TEST | CODB | - | CODE SELECT B |
| LSC | LOW SPEED COUNT | CSEL | - | CCU SELECT |
| LFS | LETTERS FIGURES STROBE | DB1 | - | DATA BIT 1 (2, et through 8) |
| MES | MESSAGE | DC | - | DATA CONTROL |
| NADV | NOT ADVANCE | DR | - | DATA REQUEST |
| NOT | NOT OUT OF TAPE | DR1 | - | DATA REQUEST INHIBIT |
| NRSS | NOT REMOTE CONTIN. STEP | DS | - | DATA STROBE |
|  | STROBE | DSS |  | SHIFT L/F GENERATOR |
| NOA | NOT OPERATOR ALARM | EB1 | - | ECHO BIT 1 (2, etc through 8) |
| NAST | NOT ALARM STOP | ECOE | - | ECHO ERROR |
| NAR | NOT AUDIBLE RESET | EEST | - | ECHO ERROR STROBE |
| NSEL | NOT SELECT | EPC | - | ECHO \& PARITY CHECk |
| NDTM | NOT DISPLAY TAPE MOTION | ERB | - | ERROR RESET B |
|  | FAILURE | FDR | - | FIRST DATA REQUEST |
| NRSR | NOT REMOTE CONTINUOUS STEP | FLT1 | - | FAULT 1 |
|  | RESET | FLT | - | FAULT 2 |
| NUL | NULL | FLTS | - | FAULT S |
| NCAN | NOT CANCEL | IDR | - | INTERNAL DATA REQUEST |
| NTMS | NOT TAPE MOTION STROBE | IDS | - | INTERNAL DATA STROBE |
| OSC | OSCILLATOR | INDP | - | INDEPENDENT |
| OS - | OFFSET SOLENOID | INH1 | - | INHIBIT 1 |
| OSD | OFFSET SOLENOID DRIVE | INH | - | UNIVERSAL KYB INHIBIT |
| PRO | PILOT HEADER OPEN | ISEL | - | INTERNAL SELECT |
| PHC | PILOT HEADER CLOSED | ITA1 | - | ITA BIT 1 (2, etc through S) |
| PH - | PILOT HEADER | IUKE | - | INHIBIT UK ENABLE |

Change 8 3-16.1
d. Type N-1 Module. Two type $\mathrm{N}-1$ gates are located on each type $\mathrm{N}-1$ module (fig. 3-14). These gates may be inverting OR gates for high inputs (case A) or inverting AND gates for low inputs (case B). The type $\mathrm{N}-1$ gates may also act as simple inverters (case C). This is accomplished by tying all input terminals together. Open circuit inputs are equivalent to low levels.
e. Type N-2 Module. One type N-2 gate is located on each type $\mathrm{N}-2$ module (fig. 3-15). This gate may be an inverting OR gate for high inputs (case A) or an inverting AND gate for low inputs (case B).
f. Type N-S Module. Two type N-3 gates are located on each type $\mathrm{N}-3$ module (fig. 3-16). These gates may be inverting OR gates for high inputs (case A) or inverting AND gates for low inputs (case B). The type $\mathrm{N}-3$ gates are used with an expander input supplied by type E-1 OR gates for case A and by type E-1 AND gates for case B. Open circuit inputs are equivalent to low levels.
g. Type 0-1 Module. Two type 0-1 gates are located on each type $0-1$ module (fig. 3-17). These gates may be noninverting OR gates for high inputs (case A) or noninverting AND gates for low inputs (case B). The type 0-1 gates may also act as simple buffers (case C). This is accomplished by tying all input terminals together. Open circuit inputs are equivalent to low levels.
h. Type 0-\$ Module. Two type 0-3 gates are located on each type 0-3 module (fig. 3-17). These gates may be noninverting OR gates for high inputs (case A) or non-inverting AND gates for low inputs (case B). The type $0-3$ gates are used with an expander input supplied by type E1 OR gates for case A and by type El AND gates for case B. Open circuit inputs are equivalent to low levels.
i. Type FF-1 Module. One type FF-1 flip-flop is located on each type FF-1 module ffig. 3-17.
(1) In the case A configuration, the flip-flop can be : let by either a high level at the $S$ input or a high level at the $J$ input which is clocked by a negative step at the CL input. The flip-flop can be cleared by either a high level at the $C$ input or a high level at the $K$ input which is clocked by a negative step at the CL input. The clocked inputs are inoperative unless the J and K inputs are low.
(2) In the case B configuration, terminals 4,5 , and 7 are tied together to form a Tinput.

When the $S$ and $C$ inputs are low, the flip-flop is toggled between the set and clear states by negative steps at the T input. Otherwise, the flipflop is set by a high level at the S input and cleared by a high level at the C input.
(3) Open circuits at the $\mathrm{J}, \mathrm{K}, \mathrm{CL}$, or T inputs are equivalent to high levels. Open circuits at the S or C inputs cause intermittent erroneous changes of state.
(4) Unused J and K inputs are wired to terminal 1 (O volt). To permanently enable J, K, or CL inputs, these inputs are wired to terminal 6 ( +4.5 volts).


Figure 3-11. Type A-1 module, logic symbols.


Figure 3-12. Type A-2 module, logic symbols.


Figure 3-13. Type E-11 module, logic symbols.



CASE A


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Figure 3-15. Type N -2 module, logic .symbols.

Figure 3-14. Type N-1 module, logic symbols.


CASE A


CASE 8 TM7440-215-15-20

Figure 3-16. Type N -3 module, logic symbols.



CASE A


CASE B


CASE B
A. TYPE O-I MODULE
B. TYPE 0-3 MODULE

C. TYPE FF-1 MODULE

D. LATCH

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Figure 3-17. Type 0-1, 0-3, FF-1, and latch module, logic symbols.

## 3-20. Integrated Circuit Latch

a. A special combination of $\mathrm{N}-1$ OR gates called a latch (fig. 3-14) is used extensively in the punched tape reader logic circuits. The latch functions as a flip-flop to register the occurrence of momentary signals. The two OR gates which make up the latch are called the set and clear sides of the latch. The 1 output of the latch which goes high when the latch is set is produced by the set side and the 0 output which goes low when the latch is cleared is produced by the clear side of the latch.
b. To set the latch, both inputs to the clear side must be low, and a high level must occur at either of the two inputs to the set side. The resulting low output of the set side then causes the clear side to produce a high level on the 1 line.

This high level reinforces the external input to the set side so that even if the external input goes low, the latch remains set.
c. To clear the latch, both inputs to the set side must be low and a high level must be applied-ther clear side input, This action causes the ' output to go low and the O output to go high. Thus, the clear condition is reinforced and remains even after the high level to the clear side goes low again.

## 3-21. Discrete Circuit Logic Elements

a. Several types of discrete circuit logic elements are described in paragraph 3-22. Each discrete circuit logic element consists of a combination of standard circuit components such as resistors, diodes, etc. Thus, wire terminal numbers
for inputs and outputs are not assigned as for integrated circuit logic elements.
b. Reference designations for discrete circuit logic elements are (A), (B), (C), etc., prefixed by the reference designation of the printed circuit card on which they are located.

## 3-22. Operation of Discrete Circuit Logic Elements

The logic operation of each discrete circuit logic element type is described below. Logic symbols for each type are given, using typical tagging lines. The logic elements are grouped by the PC card on which they are located. Schematic diagrams and detailed circuit operation of each type of discrete circuit logic element are given in baragraphs 3-74 through 3-77
a. PC Card A4. The following discrete circuit logic elements are located on PC card A4 (fig. 3-18.
(1) Type XMTR-IA. The type XMTR-1A interface transmitter converts a low level input from the punched tape reader to an open circuit for
the CCU and a high level input to 0 volt for the CCU.
(2) Type XMTR-1B. The type XMTR-1B interface transmitter transmits 0 volt to the CCU when both inputs are high. When one or both inputs go low, an open ckt is sent to the CCU
(3) Type RCVR-1A. The type RCVR-1A interface receiver converts a 0 -volt input from the CCU to +4.5 volts and an open circuit input from the CCU to 0 volt.
(4) Type RCVR-I1B. The type RCVR-1B interface receiver converts a 0 -volt input from CCU to +4.5 volts and an open circuit input from the CCU to 0 volt.
(5) Type RCVR-2. The type RCVR-2 interface receiver converts a +6.2 -volt input from the CCU to +4.5 volts and a 6.2 volt input to 0 volt.
b. PC Card A5. PC card A5 contains a single type of discrete circuit logic element. This is the type XMTR2 interface transmitter (fiq. 3-18) which transmits +6.2 volts to the CCU when both inputs are high. When one or both inputs go low, -6.2 volts is transmitted to the CCU.

## 3-22.1 Microcircuit Logic Elements

a. Lamp driver circuits used in the punched tape reader consist of thick film circuit components encapsulated within a square plastic case. These circuits are type SM-63 microcircuits, and are wired to the printed circuit cards through 10 terminals ( 1 through 10). Reference designations of the microcircuit modules are Z1, Z2, Z3, etc.. Each module contains three separate circuits. These circuits are shown separately on the logic diagrams and are designated as $\mathrm{A}, \mathrm{B}, \mathrm{C}$, etc. (For example)le: Z1A Z1B, Z1C.) The output terminal from the A circuit is always terminal I; for the B circuit, terminal 3, and for the C circuit, terminal 5 (flg. 3-18.1).
b. Power supply inputs to the individual microcircuit modules are not shown on the logic diagrams since there is no provision for them in logic symbology; however, all lamp driver (SM63) microcircuit modules receive power supply inputs of +12 volts at terminal $7,-12$ volts at terminal 8 , and ground at terminal 10.
c. The lamp driver provides a current return path for indicator lamps. One side of the indicator lamp is connected to +15 volts ac and the other side is connected to the output terminal of the lanmp driver. With no input ( O volts) to the lamp driver, an internal resistor provides a high resistance path to ground to maintain a warming current on the lamp even though it is not lit. When a high logic level is applied to the input to the lamp driver, the output terminal becomes a low resistance, high current path to ground for the lamp, and the lamp lights.
d. Terminal 9 of all lamp driver modules is wired to 1,AMIP TEST switch A3Z4 which applies +12 volts de to the lamp driver module -when actuated. This switches the lamp driver on to light the associated lamp.

## 3-22.2 Transmitter and Receiver Microcircuit Logic Elements

Some models of the punched tape reader use thick film microcircuits as interface transmitters and receivers on PC cards A4 and A-). The microcircuits are constructed similar to the microcircuit lamp drivers (para. 3-22, 1) but are wired to the printed circuit board through 14 terminals ( 1 through 14). Four types of transmitter and receiver microcircuits are supplied. Operation of each type is described as follows:
a. Type Polar Transmitter. Polar transmitters convert a 0 volt logic level to a -6 volt output, and a +4.5 volt input to a +6 volt output. Provisions are made to AND up to three input signals to the polar transmitter. When


TM7440-215-15-Cl-1
Figure 3-18.1. Micro circuit lamp driver logic symbol.
this option is used, all inputs must be high before +6 volts is transmitted. When one or more inputs are low, 6 volts is maintained at the output. Five slightly different variations of polar transmitter microcircuit modules exist, because of different output rise and fall time characteristics and number of inputs that may be ANDed together. Inputs are ANDed by applying the signals to terminals of the microcircuit module designated as diode inputs. If the input signal is applied to the direct input terminal, the output signal switches between -6 and +6 volts as the input signal varies between 0 and +4.5 volts, as described previously. Each type of polar transmitter is identified by the basic type number (T00023) and a dash number. Power supply inputs, and input and output terminals for each dash number polar transmitter is shown below. A dash in the chart indicates no connection for that function. Terminals not listed are not used.

|  | Terminal Number |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  | T00023 |  |  |  |  |
| Function | -001 | -002 | -003 | -004 | -005 |
| Direct input --------- | 14 | 14 | 14 | 14 | 14 |
| Diode input 1------- | 2 | 2 | - | 2 | - |
| Diode input 2------- | 3 | 3 | - | - | - |
| Diode input 3------- | 12 | - | - | - | - |
| Output --------- | 8 | 8 | 8 | 8 | 8 |
| + 12 volt dc supply - | 13 | 13 | 13 | 13 | 13 |
| -12 volt de supply-- | 1 | 1 | 1 | 1 | 1 |
| Ground ------------ | 7 | 7 | 7 | 7 | 7 |

b. Type T00024 Polar Receiver. Polar receivers convert a +6 volt input to +4.5 volts and a -6 volt input to 0 volts. Provision is also made to allow the receiver output to be clamped to the 0 volt output level by applying a high level on
the inhibit input. Two variations of polar receiver microcircuit module are supplied. One (T00024-001) contains two separate but identical circuits inside the module while the other (T00024-002) contains a single receiver circuit. Power supply and input and output connections for the polar receivers are shown below. A dash in the chart indicates no connection for that function. Terminals not listed are not connected.

|  | Terminal Number T00024 |  |
| :---: | :---: | :---: |
| Function | -001 | -002 |
| Input No. 1 ---------------- | 1 | 1 |
| Output No. 1 -------------- | 11 | 11 |
| Inhibit No. 1 --------------- | 13 | 1 |
| Input No. 2 ---------------- | 7 | - |
| Output No. 2--------------- | 9 | - |
| Inhibit No. 2 -------------- | 2 | - |
| + 12 volt dc supply-------- | 12 | 12 |
| - 12 volt de supply---------- | 6 | 6 |
| +4.5 volt dc supply--------- | 10 | 10 |
| Ground---------------------- | 4 | 4 |

c. Type T00121 Neutral Receiver. Neutral receivers convert a 0 volt input from the CCU to +4..) volts and an open circuit input to 0 volts. In addition, some variations of the microcircuit neutral receivers have provisions for maintaining the output at 0 volts by application of a separate inhibit signal. Four variations of neutral receiver microcircuits are supplied, with the differences being in the number)er of separate circuits contained in each module and inhibit levels used. Microcircuits T00121-001 and -002 contain three similar, but separate, receiver circuits, while T00121-003 and 004 modules contain only two. The T00121-002 and 004 modules also provide connections for inhibit signals. Inhibit A requires a high level to clamp the output to 0 volts, and inhibit B requires a low level ( O volt) signal to maintain the 0 volt output. The chart below show-s input, output, and power supply connections for the neutral receivers. A dash in the chart indicates no connection for that function. Terminals not listed are not connected.

|  | Terminal Number T000121 |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Function | -001 | -002 | -003 | -004 |
| Circuit 1: |  |  |  |  |
| Direct input---------- | 14 | 14 | 14 | 14 |
| Diode Input------------ | 12 | - | - | - |
| Inhibit $A^{\text {a }}$ - |  | - | - |  |
| Inhibit B ${ }^{\text {b-a }}$ | - | 3 | - | - |
| Output------------------ | 8 | 8 | 8 | 8 |

Terminal Number

|  | T000121 |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Function | -001 | -002 | -003 | -004 |
| Circuit 2: |  |  |  |  |
| Direct input---------- | 13 | 13 | 13 | 13 |
| Diode Input----------- | 2 | - | - | - |
|  | - | - | - | - |
| Output------------------ | 10 | 10 | 10 | 10 |
| Circuit 3: |  |  |  |  |
| Diode input------------ | 9 | 9 | - | - |
| Output-------------. | 6 | 6 | - | - |
| + 12 volt dc supply | 11 | 11 | 11 | 11 |
| - 12 volt dc supply | 1 | 1 | 1 | 1 |
| +4.5 volt dc supply--- | 7 | 7 | 7 | 7 |
| Ground | 5 | 5 | 5 | 5 |

a. Requires high level to inhibit.
b Requires low level to inhibit.
d. Type T00122 Neutral Transmitter. Neutral transmitters convert +4.5 volt logic levels to 0 volts for transmission and low level inputs to an open circuit. Four variations of neutral transmitter are supplied, with each having two or three similar, but separate, circuits and diode inputs which may be connected to provide an AND function for input signals. The following chart lists the input, output, and power supply connections for the neutral transmitters. A dash in the chart indicates no connection for that function. Terminals not listed are not connected.

|  | Terminal NumberT000122 |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Function | -001 | -002 | -003 | -004 |
| Circuit 1: |  |  |  |  |
| Direct input----------- | 13 | 13 | 13 | 13 |
| Diode Input----------- | 2 | 2 | - | 2 |
| Diode Input----------- | 3 | 3 | - | 3 |
| Output------------------ | 1 | 1 | 1 | 1 |
| Circuit 2: |  |  |  |  |
| Diode input ---------- | 10 | - | - | - |
| Diode input----------- | 11 | - | - | - |
| Output----------------- | 5 | - | - | - |
| Circuit 3: |  |  |  |  |
| Direct input----------- | 8 | 8 | 8 | 8 |
| Diode input----------- | 9 | 9 | - | - |
| Diode input----------- | 6 | 6 | - | - |
| Output---------------- | 7 | 7 | 7 | 7 |
| + 12 volt dc supply-- | 12 | 12 | 12 | 12 |
| - 12 volt dc supply--- | 14 | 14 | 14 | 14 |
| Ground----------------- | 4 | 4 | 4 | 4 |

e. Connection of Transmitter and Receiver Mlicrocircuit Modules. Transmitter and receiver microcircuit modules are connected through 14 terminals. Figure 5-1.2 shows the location of these terminals.

B. PC CARD A5 INTERFACE TRANSMITTER

TM 7440-215-15-23
Figure 3-18. PC cards A4 A5 and discrete circuit logic element symbols.

## 3-23. Ac Circuits

(fig. 8-3)
The ac input circuit receives the external ac power and distributes the power to the various circuits of the punched tape reader. The 120 -volt single-phase input power is routed through power filters FL1 and FL2 in filter assembly FL1 to power supply PS1 terminal board TB1 and (when power supply PS-2 is used), through power filters FL3 and FL4 in filter assembly FL1 to power supply PS2 terminal board TB1. The filters eliminate high frequency noise from the ac input. The power supplies provide power for identical punched tape reader component chains. The components associated with power supply PS1 will be discussed. The ac power is switched through power supply PS1 to cabinet blower B1 and to reader mechanism assembly A2. Switching control to PS1 is provided by AC POWER pushbutton Z2 on
control panel As. rower supply PS1 produces a 24 -volt de output which, when returned through the closed contacts of AC POWER switch-indicator Z2 and sequence module A12 in the power supply, turns on ac power to reader mechanism assembly A2 drive motor and cabinet blowers. When power is turned on the 24volt de output turns on the indicator in AC POWER pushbutton Z2. The power supply also provides 15 -volt ac power for illuminating the various indicator lamps on control panel A3.

## 3-24. Dc Circuits

$$
\text { fig. } 8-3
$$

The de voltages required by the punched tape reader are generated in the power supply. The following regulated voltages are supplied: +12 volts dc, -12 volts dc, +4.25 volts dc and -48 volts dc. These voltages are automatically turned
on in a specific sequence, as controlled by a sequencing module in the power supply, in order to supply bias voltages to circuit elements in such a way that no damage is done to these elements. Also, in case of a failure in any one of the dc supplies, or when the equipment is turned off, the power supplies are turned off in a predetermined sequence. Turn-on and turn-off of the dc power supplies are controlled by AC POWER switchindicator Z2. DC POWER indicator DS1 on the control panel indicates when the dc power supplies have been turned on. The reason for using the same switch to turn on ac and dc power is because the sequence of power turn-on requires ac power to be supplied to the drive motor and blowers before turning on the dc power supplies.

## 3-25. Power Supply, Block Diagram

The power supply consists of four similar regulator circuits, each containing overvoltage and current-limiting circuits, which provide regulated $+4.75 \mathrm{vdc},+12 \mathrm{vdc},-12$ vdc, -48 -volt dc power for the punched tape reader. Also included in the power supply is a sequencing circuit which turns on and off the regulators and the ac power to the drive motor and fans in a predetermined
manner, when the punched tape reader is started or stopped. The sequencing circuit also turns off the regulators and the drive motor and fans if there is a failure in any portion of the power supply. Fuses mounted on the front panel of the power supply protect each regulator assembly, the ac powerlines to the drive motor and fans, and the main ac power transformer in the power supply. The AC POWER switch-indicator on the control panel of the punched tape reader is used to turn the power supply on and off. The sequencing circuit lights the lamps in the pushbutton switch when the power supply is on.

## 3-26. Rectifiers and Voltage Regulators

fig. 3-19
a. The power supply receives $120-\mathrm{volt}$, $50 \mathrm{or} 60-\mathrm{Hz}$ ac power, which is applied to the primary of the main power transformer. Ac voltages from the secondary windings are applied to five fullwave rectifier and filter networks, four of which supply input dc voltages to the four regulator circuits; the fifth rectifier supplies the unregulated 24 -volt dc power required by the sequence module.
b. The four regulating circuits operate similarly; therefore only the +4.75 -vdc regulator is illustrated in figure 3-19 and described in (1) through (3) below.
(1) A nominal +10 vdc is supplied from the rectifier and filter to a series regulator circuit in the $+4.75-$ volt regulator. The series regulator, under the control of the regulator control circuit, acts as a variable resistance load which reduces the unregulated 10 volts dc to an accurately regulated +4.75 volts dc. Variations in the output voltage from this value are sensed by the voltage sensor network, which applies a corresponding control voltage to the regulator control circuit. This circuit, in turn, controls the series regulator in a way which changes the voltage drop across this circuit by the proper amount to maintain the output voltage at +4.75 volts dc.
(2) As a safety feature, an overvoltage sensor circuit and an over-current sensor circuit are included in the regulator circuits. If the output voltage momentarily rises above 115 percent of the rated output, this is sensed by the overvolt-
age sensor. A control voltage is then applied to the regulator control circuit to cause the series regulator to produce a sharp drop in the output voltage. This action should return the regulator circuit to the proper output voltage. If the overvoltage condition is due to a failure in the regulator circuit, rather than to a transient condition, it cannot be corrected by the overvoltage circuit. In this case, the excessive voltage causes the fuse at the input of the series regulator circuit to blow, protecting the regulator from further damage.
(3) If the output current rises above 120 percent of rated value, this is sensed by the overcurrent sensor, which provides a control voltage to the regulator control circuit to cause the series regulator to produce a sharp output voltage drop which practically turns off the series regulator. A corresponding severe current drop is produced. This action produces current-limiting during load faults in which the short circuit currents are less than the rated currents, effectively minimizing power dissipation at these times.

## 3-27. Power Turn-On and Turn-Off Sequencing Control <br> fig. 3-20

a. In order to minimize the initial power drain upon turn-on of the punched tape reader (by means of the AC POWER switch-indicator), and to protect the electronic circuits in the punched tape reader from damage due to the improper sequence of application of bias and control voltages when power is initially turned on, the various dc voltages required by these circuits are supplied by the power supply in a specific predetermined sequence. Also, if the punched tape reader is turned off by means of the AC POWER switchindicator, the power supplies are automatically shut down in the opposite sequence to turn-on, with certain specific delays between individual power turn-off being included. In addition, if there is a failure in any of the circuits of the power supply, the complete power supply is automatically shut down in a specific sequence, again protecting the punched tape reader circuits from damage due to improper operating voltages. The sequencing circuit also controls the turnon and turn-off of the ac power to the drive motor and the fans, assuring that this power is supplied before the various de voltages are supplied, and turning off this power when the punched tape reader is shut down or when there is a failure in the power supply. The 15 -volt ac lamp power for the AC POWER switch-indicator and the other indicators of the punched tape reader control panel are also controlled by the sequencing circuits. When power is turned off, all lamps will be dark.
b. All of the automatic power sequencing circuits are mounted on sequencing module A12, and consist basically of two types of voltage level sensors. One type senses whether each of the regulated dc output voltages is within 90 percent of rated output level and the other type senses when the output level of certain of the power supplies falls below 1.8 volt or 10 percent of rated value, whichever is higher. The 90 percent of rated value represents the minimum output voltage level at which a regulator is considered on and operating normally. During the turn-on sequence, these sensors determine when a particular regulator is on and providing the proper output voltage amplitude, and then provide the control to turn on the next regulator in the power turn-on sequence. The 90 percent sensors are also used
to sense if there is a less-than-normal output from a regulator, indicating a failure in this regulator. If this occurs the particular sensor involved initiates an automatic turn-off procedure which turns off all the regulators in the proper sequence.
c. The turn-off procedure for each regulator is a two-stage action. First the regulator output voltage is reduced to a value of approximately 10 percent of rated value (or 1.8 volt, as applicable). The regulator is then considered to be off. At a later stage of the turn-off sequence, a second control action is applied from the sequence module to the regulator to completely turn off the output voltage.
d. The operating voltage for the sequence module is supplied by the 24 -volt rectifier-filter. This voltage is converted to a regulated 15.0 volts dc, which is used as the bias and collector voltages for the transistors of the sequence module. A 90 percent fault sensor monitors the output of this regulator as part of the overall power failure monitoring control. The sequence module operates as follows:
(1) When the AC POWER switch-indicator is depressed to start operation of the punched tape reader, it momentarily applies the 24 volts dc from the 24 -volt dc rectifier-filter network to a self-latching relay in the sequence module. This action energizes the relay, which holds itself energized after the AC POWER switchindicator is released. The latching relay applies the 24 volts dc to a relay driver in the sequence module, which then energizes the ac power relay. This action
applies the auxiliary ac power to the drive motor, the fans, and to all control panel indicator lamps.

The AC POWER switch-indicator lights to indicate that the ac power is now on. In addition, the 24 volts dc is applied to the 15.0 -Nvolt dc regulator in the sequence module which produces a regulated 15.0 -volt dc output. which is required to operate the other circuits of the sequence module. This action is the start of the automatic turn-on for the four regulators. The regulators are turned on in the following sequence: 12 volt, de, +4.75 volt de, +12 volt dc, and -48 volt dc.
(2) When the output of the 15.0 -volt regulator reaches 90 percent of rated value ( 12 volts dc), the + 15.0 -volt 90 percent sensor applies a bias voltage to the series regulator of the 12 -volt. regulator circuit. Until this bias is applied, the regulator circuit is disabled and produces no output. A sample of the outputs of all the regulators are applied to individual 90 percent sensors on the sequence module. Thus, when the output of the --12 -volt regulator builds up to at least 90 percent of rated value ( -10 volts de), the -12 -volt 90 percent sensor applies a turn-on bias to the +4.75 -volt regulator, to turn on this regulator. This action continues, with the applicable 90 percent sensors applying a turn-on bias to the corresponding voltage regulator.
(3) The turn-off sequence is started by again pressing in the AC POWER switch-indicator. This action applies the 24 -volt dc power to a pulse generator which produces a pulse which is applied to the overvoltage sensor circuit of the -48 -volt regulator to cause this circuit to sharply reduce the output voltage of the -48 -volt regulator. When the output voltage drops to 10 percent of rated value, or less, the regulator is considered to be off. A -48-volt 10 percent voltage sensor senses that the voltage has dropped to the off amplitude and it applies a gate voltage to the overvoltage sensor circuit in the $+12-$ volt regulator to turn off this regulator. As the output voltage of the +12 -volt regulator now drops below 90 percent of rated value, this is sensed by the +12 -volt 90 percent sensor. The sensor now removes the series regulator bias from the -48 -volt regulator circuit (previously turned off to less than 10 percent of rated output), completely turning off the 48 -volt regulator. As the output of the +12 -volt regulator continues falling to 10 percent of rated value, the +12 -volt 10 percent level sensor senses this condition and applies a gate voltage to the overvoltage sensor circuit, of the +4.75 -volt regulator. This action turns off the +4.75 -volt regulator. The action continues in a manner similar to that previously de
scribed in the following sequence. The +4.75 -volt 90 percent sensor turns off the +12 -volt regulator completely. Then the +4.75 -volt 10 percent sensor applies a voltage to the relay driver clamp, which deenergizes the ac power relay removing the ac power from the drive motor and fans. At the same time, the voltage from the +4.75 -volt 10 percent sensor is applied to a $300-\mathrm{ms}$ timer. Approximately 300 -nls later, the timer circuit operates a pulse generator which generates a pulse to turn off the -12 -volt regulator. The 12 -volt 90 percent sensor then completely turns off the +4.75 -volt regulator. The pulse produced by the pulse generator is also applied to the turn-off control for the latching relay. The. turn-off control then deenergizes the relay, interrupting the 24 -volt de power applied to the +15.0 -volt dc regulator. This completes the sequenced power turnoff procedure.
e. If there is a failure on any of the power supplies, the complete power supply is automatically shut down in a predetermined sequence which is somewhat different from the normal shut down sequence. A regulator is assumed to have failed if its output voltage drops to 90 percent or less, of rated output. If the -48 -volt, +12 -volt, or +4.75 -volt supply fails all of these three supplies are turned off simultaneously and then, after the same 300 ms time delay required for the normal turn-off procedure, the -12-volt supply is turned off, as is the ac power and the regulator +15.0 -volt supply. If the -12 -volt supply has failed, the other supplies are turned off simultaneously and almost immediately, and if the 15 -volt regulator in the sequence module fails, this initiates turn-off of the 12 -volt supply to produce complete power shutdown. A failure in a supply is sensed by the 90 percent sensor associated with that supply. The sensor then operates a silicon control rectifier (SCR) driver to initiate turn-off by firing the associated SCR in the applicable regulator. A single SCR driver is controlled by any one of the 90 percent sensors for the four regulators, and this SCR turns off the -48 -volt, -+4.75 -volt, and +12 -volt regulators simultaneously. The -12 -volt regulator is then turned off in the normal manner, as previously described.
$f$. The SCR driver used for turn-off if a failure is detected must be prevented from operating during power turn-on. This is accomplished by the driver clamp timer and driver clamp circuit, which inhibits the SCR driver for a period of 1.8 second after the start of power turn-on. The
same circuit inhibits the operation of the 10 percent sensors during turn-on, since these sensors would also interfere with the turn-on sequence. During the normal turn-off sequence the SCR driver must again be inhibited otherwise it would interfere with the normal turn-off sequence. This is accomplished by the 80 ms timer.

## 3-28. Detailed Circuit Description of Rectifiers and Voltage Regulators (fig. 8-4

a. Input Rectifier Circuits. The power supply receives $115-$ volt, 50 or $60-\mathrm{Hz}$ ac power at terminals 1 and 2 of terminal board TB1. A 10-ampere fuse, A10 F5, is included in the line from the terminal board to the primary of transformer A9TI,The secondary of this transformer provides ac voltages to four full-wave rectifiers. The full-wave rectifiers are as follows: Diodes A4CR4 and A4CR3, with filter capacitor A9C6, provide a nominal -68-volt dc input to the 48 -volt de regulator circuit. Diodes A5CR3 and A5CR4, with filter capacitor A9C5, provide a nominal -2Cllt dc input to the -12 -volt dc regulator circuit. Diodes A5CR1 and A5CR2 and filter capacitor A9C4 provide a nominal +20 -volt dc input to the +12 -volt dc regulator circuit. Diodes A4CR1 and A4CR2, with filter capacitors A9C2 and A9C3, provide a nominal +10 -volts dc for the +4.75 -volt dc regulator.
(1) A pair of ac outputs are picked off taps 9 and 7 and 5 and 7 of the secondary of transformer A9TI to provide 15-0-15-volt ac power for the indicator lamps of the punched tape reader. Fuses A10 F9 and AIOF10 are included in each line to protect the transformer from an overload. The application of the 15 -volt ac lamp illumination power is controlled by relay A9K1, as is the ac power to the drive motor and fan. The relay is energized by the sequence module as part of the power turn-on procedure.
(2) A second output winding, taps 12 and 13 on the transformer, provides a nominal 23volt ac input to a full-wave bridge rectifier, A15CRI, CR2, CR3, CR4, and filter capacitor A9C1 which provides a nominal 24 -volt dc input to the sequence module (para 3-29).
b. $\quad+4.5-$ Volt Dc Regulator Circuit
(1) Voltage regulation. The unregulated 10 volt-dc output of rectifier A4CR1 and CR2 is applied through fuse A1OFX1 to the series regulator consisting of transistors A4Q1 and Q2 con-
nected in parallel. The transistors act as a variable resistance in series with the 10 volts de to drop this voltage to +4.75 volts at the output of the regulator (junction of A4R1 and R2). The regulator control circuit senses variations in the output voltage from +4.75 volts and adjusts the voltage drop across the series regulator transistors to compensate for these variations, thus maintaining a +4.75 -volt dc output.
(a) The 10 volts de is applied to the collectors of transistors A4Q1 and Q2 connected in parallel. The voltage drop across the transistors is controlled by the base voltage applied to the transistors, which is supplied by the regulator control circuit. The outputs of the two transistors are taken from their emitters and coupled through emitter resistors A4R1 and R2, respectively to a junction point and to the regulator output terminal, pin 2 of TB2. The resistors provide emitter degeneration to assure satisfactory current sharing between the two series regulator transistors.
(b) Zener reference diode A1CR6 provides a regulated voltage to a voltage divider consisting of A1R23, A1R24, and A1R25, which provides a fixed bias to the base of A1Q5 (part of differential amplifier A1Q5 and Q6). A sample of the output voltage of the regulator is applied to the base of Q6. The wiper arm of potentiometer A1R24 is set so that during the stable condition of the regulator the proper voltage is picked off this voltage divider to operate the regulator circuit to provide a +4.75 -volt dc output. Should the output voltage vary from this value, the voltage at the base of Q6 increases or decreases proportionately, producing a corresponding variation in the output voltage of Q6. Since the base of A1Q5 is held at a constant voltage by Zener regulator diode A1CR6, the common emitter of Q5 and Q6 is held at a voltage which only varies with variations in transistor characteristics or variations in bias. However, since transistors Q6 and Q5 are of the same type, temperature variations, bias voltage variations, aging and other variations of this type have the same effect on both transistors and there is no net change in the base-to-emitter voltage at Q6. Only a change in the base voltage at Q6 produces a net change in the collector voltage at Q6. The voltage at the collector of Q6 is applied to the base of AIQI. If there has been an increase in the regulator output voltage above 4-4.75 volts, the voltage ap-
plied to Q1 decreases, decreasing the voltage at the base of emitter follower A4Q3, which reduces the voltage at the parallel bases of series regulators A4Q1 and Q2. The voltage drop across these transistors increases, reducing the output voltage back down to +4.75 volts dc. A similar analysis applies if the output voltage has fallen below +4.75 volts dc.
(c) The emitter follower stage A4Q3 is used as a current amplifier to provide adequate current amplification for the series regulator.
(2) Current limiting. The sum of the currents at the emitters of series regulators A4Q1 and Q2 is the output current of the voltage regulator. Parallel connected resistors A1R4 through R9 comprise a summing network which samples this current and provides a proportional voltage at the base of Q4. By biasing diode A1CR4 in a forward direction the net baseemitter threshold voltage for Q4 is set to cut off Q4 during normal operation. The use of diode CR4 to establish base bias provides temperature stabilization and permits operation at low signal levels. If the load current on the series regulator increases to 120 percent of rated value, the voltage drop across current-sensing resistors A1R4 through R9 increases sufficiently to turn on A1Q4. This causes a sharp voltage drop at the collector of Q4, which is connected to the base of Q1, producing a corresponding voltage drop at the base of. Q1 which severely reduces the conduction of series regulators A4Q2 and Q1. This action causes a sharp decrease in output voltage, further forward-biasing A1Q4, and reinforcing the current-limiting action. As a result, current-limiting occurs at lower load currents. This type of current control, where the current reference is a function of the output voltage, results in short circuit currents that are less than rated currents, which minimizes power dissipation in the series regulator stage during load faults.
(3) Overvoltage protection. Zener reference diode A1CR5 provides a constant voltage to a voltage divider consisting of A1R29, A1R30 and A1R31, which provides a fixed bias to the base of A1Q7. Transistor A1Q7 is part of differential amplifier A1Q7 and A1QI. A sample of the output voltage is applied to the base of A1Q5. The wiper arm of potentiometer A1R30 is adjusted so that with normal output voltage A1Q8 is cutoff because of
the emitter bias across common emitter resistor A1R35. With A1Q8 cutoff, the base of A1Q9 is at supply potential and A1Q9 is also cutoff. If the output voltage should exceed the normal value of 4.75 volts by 115 percent ( 5.5 volts), the portion of the voltage coupled to the base of A1C causes A1Q to conduct. The voltage drop across collector load resistor A1R34 lowers the base bias on A 1 Qg , driving it into conduction, When A1Q9 conducts it applies a positive level to voltage divider A15R5,A15R6 which fires silicon control rectifier A14CR2, causing the diode to conduct heavily and drop the rectifier output voltage to a low level.
(4) Overcurrent Protection. 'The overcurrent protection transistor A1Q4 operates at a relatively small positive voltage level in the 4.75 -volt supply, since this is the level of the output voltage being monitored. As a result, because of transistor characteristics the bias levels are insufficient to guarantee that the transistor will actually turn on if an overload condition is reached. To assure that the transistor turns on, it is supplied with a regulated negative bias from emitter follower AIQ3, which is connected to regulator Zener diode AICR1. The negatives bias supplied is approximately -11.5 volts. This same bias is supplied to the +12 -volt supply but is not required by the negative voltage regulators.
c. Turn-On and Turn-Off. The regulator circuit is automatically turned on and/or turned off by the sequence module, A12. Turn-on is accomplished by the sequence module, which turns on a transistor whose collector is connected to pin W of A9J4. Before turn-on by the sequence module, an open circuit exists at pin W and A1Q2 cannot conduct. When the transistor in the sequence module is turned on, it provides a ground at pin W and current now flows through A1CR2 and CR3 and transistor Q2 is driven to the conduction state. This action produces a base bias for Q1 and collector bias for Q6. The base bias for Q1 causes it to conduct and produce a current source for A4Q3 which then turns on the series regulator A4Q1 and Q2. Turn off is accomplished by firing the over-voltage protection SCR A14CR2 thus dropping the output voltage to near zero. Refer to paragraph 3-29 for a description of the operation of the sequencing module. Diodes A1CR2 and A1CR3 provide protection
for transistor A1Q2 against excessive back bias.
d. Other Regulator Circuits. The -8 vdc regulator, +12 vdc regulator, and -12 vdc regulator operate in a manner similar to the +4.75 volt regulator. The differences are as follows:
(1) In the -48 -volt supply, transistor A3Q4 controls the turn-on in response to the switching action in the sequence module. To turn on the -48 -volt supply, a bias level of approximately +15 volts is applied at pin N of A9J4 to the emitter of Q4. This supplies a current source to the series regulator in A6. Current overload protection is provided by current sensor A6R2 and current overload transistor A3Q1. If there is a current overload, $A 3 Q 1$ is turned on, reducing the negative voltage level at the collector of Q1, turning on Q2. This turns off the regulator stage, dropping the output voltage, as described for the +4.75 -volt regulator. Normal voltage regulation is provided by differential amplifier A3Q6, Q7 which controls regulator control transistor A3Q3, through voltage splitter Q5. Transistor Q5 permits lower bias levels to be used than those normally available from the relatively high voltage levels which exist in the -48 -volt supply.
(2) For the -12 -volt supply, turned-on control from the sequence module consists of supplying a bias of approximately +15 volts at pin V of A9J4 to transistor A2Q8, turning it on. This supplies the required current source to the -12volt series regulator. Other circuit operations are the same as for the +4.75 -volt supply previously described.

## 3-29. Detailed Circuit Description of Sequence Module (A12) <br> fig. 8-5

The sequence module turns the complete power supply on and/or off in a predetermined manner when the AC POWER switch on the control panel is operated. Also, the failure of any one regulated output turns off the remaining outputs in a proper sequence.
a. Input Circuit and Ac Relay Control. The 24volt dc full-wave rectifier on module i15 supplies unregulated 24 vdc power to the normally open contacts of relay K1 on the sequence module, and to the AC POWER switchindicator on the punched tape reader control panel. When this switch-indicator is operated, its contacts are momentarily closed, applying the 24 vdc through
diode CR21 and resistor R60 to the coil of relay K1, energizing it. The relay is then latched on by the 24 vdc through its now closed contacts, through diode CR32 and resistor R60. Thus, this relay stays energized when the AC POWER switch is released. The voltage applied to the coil of relay K1 is also applied to the base of Q1, which turns it on, causing it to conduct current. This action energizes the auxiliary ac power relay, A9K1 (shown on the regulator circuit), applying the auxiliary 115 vac power to the fans, the drive motor, and the AC POWER lamp and the other indicator lamps.
b. Voltage Regulator. The unregulated 24 vdc power is coupled through the contacts of energized relay K1 on the sequence module to the 15 volt regulator. The regulator converts the unregulated 24 -volt dc power to regulated 15.0 -volt dc power. The 24 volts is applied to series regulator Q33, which acts as a variable load in series with the input voltage, varying its internal impedance to maintain the output voltage at +15.0 vdc. The series regulator is controlled in the following manner:
(1) The output voltage of the regulator is developed across voltage divider R72, R73 and R74. Capacitor C10 removes high frequency variations on this voltage. Potentiometer R73 is adjusted to obtain the required +15.0 -volt output when the overall control loop is stabilized. Should the output voltage tend to change from +15.0 volts, the voltage applied to the base of Q35 changes proportionately. The emitter of Q35 is held at a constant voltage by Zener regulator diode CR27 so that only a variation in base voltage can cause a change in collector voltage of Q35. The voltage change at the collector of Q35 is applied to the base of emitter follower Q32, which, in turn, changes the voltage at the base of Q33. This action varies the voltage drop across Q33 proportionately, returning the output voltage to the required level. For example, an increase in the output voltage produces an increase in the voltage at the base of Q35, which results in a subsequent decrease in the voltage at the base of Q32 and Q33. This increases the voltage drop across Q33, lowering the output voltage to the required value. Transistor Q31 is connected from the base to collector of Q32 and acts as a shunt path for base current of Q32. In this manner Q31 tends to maintain a constant current source at the base of Q32, minimizing excessive current variations through the series regulator.
(2) For normal output currents, transistor Q34 is reverse biased by voltage divider R67 and R68 and is cut off. If the output current rises above approximately 500 ma , a sufficient voltage drop is developed across resistor R69 to overcome the back bias on Q34, causing it to conduct. This creates a shunt path for the output current, limiting the output current to a maximum of 500 ma.
c. Turn-On Sequence. After latching relay K1 has been energized, causing the voltage regulator to provide the regulated +15.0 -vdc output, the regulators are turned on automatically as follows: $-12 \mathrm{vdc}, \mathrm{t} 4.75 \mathrm{vdc},+12 \mathrm{vdc}$, and -48 vdc . The sequence module performs this turnon action as follows:
(1) -12 volt turn-on. The +15.0 -vdc output of the +15 -vdc regulator in the sequencing module is applied to voltage divider R89 and R80. The voltage at the junction of R89 and R80 is applied to the base of Q39 whereas a reference voltage from Zener diode CR30 is applied to the emitter of Q39. The reference voltage keeps Q39 cut off until the voltage applied to voltage divider R89 and R80 reaches a level of at least 12 volts dc. This occurs after the 15 -volt regulator has been turned on and reaches 90 percent of rated output. Conduction of Q39 drives Q38 into conduction, providing the bias voltage required to operate the series regulator in the -12 volt regulator. This turns on this regulator. The collector of Q39 is at approximately -24 volts dc before it is turned on and at approximately +15 volts dc after it is turned on.
(2) -12-volt output sense ( 90 percent). A sample of the output of the -12-volt regulator is applied to the base of transistor Q36 of differential amplifier Q36, Q37. Voltage divider R75 and R76, connected across the output of the 15.0 volt dc regulator, provides a reference voltage to the base of Q37, The output at the common emitter of Q36 and Q37 keeps Q36 cut off until the -12 -volt regulator output reaches at least -10.80 volts. When the output of the -12 -vdc regulator exceeds the 10.80 volts, Q36 is driven into conduction. The collector of Q36 is connected to the +4.75 -vdc regulator turn-on circuit, to control turn-on of this regulator.
(3) +4.75 volt turn-on. When Q36 is driven into conduction, its collector goes from approximately +15 volts de to -3 volts de causing Q21 to conduct. This, in turn, causes Q18 to
conduct, providing the turn-on bias to the series regulator of the +4.75 -volt regulator. Before conduction, the collector of Q18 is at approximately 15 volts dc and after conduction it is at approximately 0.25 volt dc.
(4) +4.75-volt, output sense ( 90 percent). A sample of the output of the +4.75 -volt regulator is applied to the emitter of Q4. The base of Q4 receives a regulated reference voltage from voltage divider R9 and R10, supplied by the +15.0 -volt regulator. When the output of the +4.75 -volt regulator reaches 90 percent of rated output ( 4.275 volts), Q4 conducts, causing its collector to go from 0 volt to approximately +4.0 volts to turn on the +12 -vdc supply.
(5) +12-volt turn-on. The conduction of Q4 causes Q5 to turn on, which provides a turnon bias to the series regulator of the +12 -volt regulator. The collector voltage of Q5 is approximately +24 volts dc prior to turnon and approximately 0.25 volt dc after turn-on.
(6) +12 volt output, sense ( 90 percent). A sample of the output voltage from the +12 volt regulator is applied to the emitter of Q9. A reference voltage, provided by voltage divider R18 and R19, from the regulated +15.0 -volt regulator is applied to the base of Q9. When the output of the +12 volt regulator reaches 90 percent of rated value ( 10.80 volts), Q9 conducts, causing its collector voltage to go from 0 volt to approximately 10 volts to turn on the -48 volt supply.
(7) -48-volt turn-on. The conduction of Q9 causes Q10 to turn on. Conduction of Q10 provides a current flow through voltage divider R16 and R17, causing Q8 to conduct. This action supplies emitter current to Q15, turning it on and it then supplies the required bias for the series regulator of the -48 -volt supply.
(8) -48 -volt output, sense. A sample of the output voltage of the -48 -volt supply is applied to the base of transistor Q29, which acts as the 90 percent sensor for the -48 -volt supply. This sensor is only used in the turn-off sequence when a fault occurs.
d. Turn-Off Sequence. When the AC POWER switch on the punched tape reader is pressed in order to turn off power, the sequence module turns off the regulators in a sequence opposite to the turn-on sequence ( (1) through (10) below).
(1) -48 -volt regulator power reduction. When the AC POWER switch is depressed, the

24 volts dc from the 24 -volt dc rectifier is applied through the momentarily closed contacts of the switch to the RC pulse-forming network of 17 and R62 and pulse transformer T1. The primary if T1 forms a pulse which is coupled to the secondary, which applies this pulse to the silicon control rectifier (SCR) overvoltage turn-off diode in the 48 -volt regulator. This reduces the output of this power supply to less than 10 percent of rated output, which, in effect, turns it off. The pulse forming network produces only a short-duration single pulse upon operation of the AC POWER switch and when the switch is released, turn-off has been initiated and continues automatically. The action of this circuit has no effect during the power turn-on sequence since the -48 volt supply is the last supply to be turned on, and the pulse forming network will have been discharged before turnon of the -48volt supply is accomplished.
(2) -48 -volt, +12 -volt, +4.75 -volt 90 percent sensor inhibit. The pulse formed in transformer T1 is coupled through a second output winding to the base of Q12. Transistors Q12 and Q13 comprise a single-shot multivibrator which produces an output pulse with a duration of 80 ms . During this time duration that the single-shot is fired, it turns on amplifier Q14, which is normally cut off, which in turn, causes Q20 to conduct. Transistor Q20 acts as a clamp, clamping the base of Q19 to a low level, through diode CR8 'during the first 80 ms of the turn-off sequence. This action inhibits the operation of Q19 during the sequenced shutdown accomplished by operating the AC POWER switch. Transistor Q19 is only used to turn off the -48-volt, +4.75 volt and +12 -volt supplies in case of a regulator failure (e below).
(3) -48-volt, output 10 percent sensor. As described in (1) above, the operation of the AC POWER switch fires the overvoltage SCR in the -48 -volt regulator, reducing the output voltage from this supply. A sample of the -48 -volt output voltage is applied to the base of Q3o. When the output of the -48-volt supply is normal, the base voltage is sufficiently negative to keep Q30 cut off. As the output of the -48 -volt supply is reduced towards zero during turn-off, the base bias will become sufficiently less negative to cause Q30 to conduct which initiates power reduction of the +12 -volt supply.
(4) +12-volt power reduction and -48-volt turn-
off. Conduction of transistor Q30 applies a
negative voltage through diode CR19 to the base of Q27, causing it to conduct. This action applies a pulse through diode CR17 of OR gate CR17, CR18 to the SCR in the overvoltage protection circuit of the +12 volt regulator, initiating turnoff of this regulator to reduce its output voltage to less than 10 percent of rated value. The 90 percent level detector, Q9, across the output of the +12 volt supply senses that the output of the +12 -volt regulator drops below 90 percent of rated value and removes the turn-on bias from the series regulator of the -48 -volt regulator, completely turning of this regulator.
(5) +12 -volt output 10 percent sensor. A sample of the +12 -volt regulator output is applied to the emitter of Q28, and the base of Q28 receives a reference voltage from voltage divider R50 and R51, connected across the 15.0 -volt regulated supply. Transistor Q28 is normally cut off by the high emitter voltage. However, during the turn-off sequence, when the output of the +12 -volt regulator drops to 1.8 volt, Q28 conducts, to initiate reduction of the output voltage of the +4.75 -volt supply.
(6) +4.75 -volt regulator output voltage reduction and +12 -volt regulator turn-off. Conduction of Q28 applies a negative voltage through diode CR15 to the base of SCR driver Q36, causing it to conduct and apply a positive voltage through diode CR13 of OR gate CR13, CR14 to the SCR overvoltage turn-off diode in the 4.75 volt regulator. This action reduces the output of the 4.75 -volt regulator to less than 1.8 volt, thus, in effect, turning it off. The 90 percent level detector (Q4) across the output of the 4.75 -volt supply senses that the voltage is below 90 percent of rated value. This results in Q5 being cut off, which removes the turn-on bias from the +12-volt regulator, to turn off this power supply completely.
(7) +4.75-volt, output 10 percent sensor -AC power turn-off. A sample of the output voltage of the +4.75 -volt regulator is applied to the emitter of Q23. The base of Q23 receives a reference bias from the voltage divider consisting of R44 aid R45 connected across the 15.0 -volt regulator. The emitter bias keeps Q23 normally cut off. When the emitter voltage drops to 1.8 volt during the turn-off sequence, Q23 is driven into conduction. This produces a voltage drop at the base of Q22, through diode CR10, causing it to conduct and apply a positive voltage of approximately 15 volts to the base-emitter voltage
divider, R2 and R3, of relay control amplifier Q2.
Amplifier Q2 now conducts heavily, reducing the base voltage on relay driver Q1 sufficiently to turn off Q1. This action removes excitation from the coil of the ac power relay A9K1, turning off ac power for the drive motor, the fans and also the AC POWER lamp and the other indicator lamps. The unlighted AC POWER lamp indicates that the ac power is turned off.
(8) -12-volt regulator voltage reduction and +4.75 -volt turn-off. The conduction of Q22 also applies +15 volts dc to the RC timer circuit of R4 and C1. During the time that the voltage builds up on C1, transistor Q3 is biased to be cut off and the voltage across C 1 is applied to SCR CR33. After approximately 300 ms , the ,-voltage across CR33 builds up to $8+1$ volts dc, at which time CR33 conducts. Conduction of CR33, causes a sharp reduction in base voltage of Q3, driving it into conduction. Capacitor C1 now discharges through Q3 and the resulting current flow through R8 to the SCR in the overvoltage protection circuit of the -12 -volt regulator causes the output voltage of the regulator to drop to less than -2 volts dc. The drop in output voltage of the -12volt supply below the 90 percent level is sensed by 90 percent level sensor Q36 and Q37 connected across the output of the -12 vol supply. This results in transistor Q21 being turned off, which removes the bias from the series regulator in the +4.75 -volt supply, completely turning off this power supply.
(9) Turn-off of -12-volt supply and power turnoff in sequence module. The discharge of capacitor C1 through transistor Q3 applies a discharge current through R7 and diode CR2, into SCR CR24 across the coil of relay K1. This voltage drop is also coupled through diode CR29 to the base of Q39. This action back-biases Q39, turning it off, which in turn, cuts off Q38, to remove the bias voltage from the series regulator in the -12-volt regulator, and completely turning off this power supply. The pulse applied to SCR CR24 fires this SCR, shorting out the coil of relay K1 (deenergizing K1). This action removes the 24 -volt dc power from the 15.0volt regulator, removing all power from the circuits of the sequencing module to complete the turn-off procedure.
(10) Transistor protection. Those level detector transistors which could be subject to relatively high reverse base-emitter voltages are protected by diodes connected between the base
and the emitter. The diodes short out excess reverse base-emitter voltages.
e. Fault Sensing and Turn-Off. If the -48 -volt, $+12-$ volt, or +4.75 -volt supply fails, the others must be turned off at the same time. After this is accomplished the -12volt supply is turned off. If the -12-volt supply fails, the other three supplies must be simultaneously turned off within 50 ms after this failure. Turn-off is accomplished by means of the 90 percent sensors which sense when the output voltage of a regulator has fallen to 90 percent, or less, of rated output.
(1) Should the +4.75 -volt regulator output fall to less than 90 percent of rated value, this is sensed by the +4.75 -volt 90 percent sensor (Q4) which turns off Q6, which in turn turns on Q7. The collector of Q7 is reduced to near ground level, applying a negative voltage through diode CR8 to the base of Q19. This action turns on Q19, providing a positive voltage through diodes CR6, CR14, CR18 to the -48 -volt SCR, the +4.75 volt SCR, and the +12-volt SCR, turning off these supplies simultaneously. Transistor Q19 is also operated by either the -48-volt 90 percent sensor (Q29), the +12 -volt 90 percent sensor (Q9, Q10, Q11) or the -12 -volt 90 percent sensor (Q36 and Q17), if any of these power supplies fail. The -48volt SCR is operated by Q19 firing SCR CR34 across pulse forming network C4 and R30. The output pulse is supplied to T1 for application to the SCR in the 48 -volt supply.
(2) After the -48 -volt, +4.75 -volt, and +12 -volt supplies are simultaneously turned off, the -12 -volt supply is turned off as previously described. If the $+15-$ volt regulator in the sequence module fails (power output drops to less than 90 percent of rated output), this is sensed by the +15.0 -volt 90 percent sensor which turns off the bias to the -12 -volt series regulator. This action turns off this regulator, initiating the previously(, sly described shutdown procedure.
f. Override Timer Circuit for Turn-On Circuit. As previously described, the turn-off circuits include sensors which operate when output voltages are below 1.8 volt dc or 10 percent of rated output, whichever is higher. In addition, the 90 percent detectors function as fault detectors if the output voltage of any regulator drops below 90 percent of rated value (e above). Both of these sensors must be inhibited during the power turnon, since they would interfere with the power
turn-on sequence. This is accomplished by the action of driver clamp Q24. When the 24 volt dc is initially applied to the 15.0 -volt regulator to produce the regulated 15 -volt output, the +15 volt output is applied to the emitter and base of driver clamp Q24, causing it to conduct, producing a positive voltage at its collector. This positive voltage is coupled through diodes CR20, CR16, CR11, and CR9 to the -48 -volt 10 percent sensor (Q30), the +12 -volt 10 percent sensor (Q28), the +4.75 -volt 10 percent sensor (Q23), and the 90 percent fault sensor line to Q19. It thus blocks diodes CR19, CR15, CR10, and CR8, preventing the 10 percent and 90 percent fault sensors from operating and turning off the power supplies. At the same time that Q24 is turned on, the +15 volts is applied to timer circuit R84 and C12. The RC time constant of this circuit is selected so that the voltage on C12 builds up to a sufficient level to turn on Q16 in approximately 1.8 second. Zener diode CR30 establishes the turn-on bias for Q16. When Q16 is turned on it supplies base current for Q25, turning it on. This produces a positive voltage at the base of Q24 which turns off Q24, removing the inhibiting voltage from diodes \%7R19, CR15, CR10 and CR8. The 10 percent sensors and 90 percent fault sensor, Q19, are no longer inhibited, since after 1.8 second all power has been turned on and the fault sensors should now operate.

## $3-30$. Voltage Regulation for +6.2 -Volt and -6.2 -Volt Dc Power

Voltage regulator circuits are located on PC card A5 ffig. 8-10) and produce 6.2-volt and -6.2-volt power for use by the receive and transmit interface circuits.
a. The -6.2 -volt power is derived from the -12 -volt source by Zener diode VR1 and resistor R91. Capacitor C11 minimizes the effect of switching transients on the -12-volt power.
b. The t6.2-volt power is derived from the ,-12-volt source by Zener diode VR2 in conjunction with resistor R92. Capacitor C0O minimizes the effect of switching transients on the A 12-volt power.

## 3-31. Power On Reset Control Circuits

When power is turned on to the punched tape reader, a reset signal is generated to clear various latches in logic assembly AI in preparation for a new read cycle. The power on reset (PRST)
signal is initiated by operation of AC POWER pushbutton on control panel A3 (para 2-1)] When this pushbutton is pressed, -48 volts dc is applied to the power on reset circuit on PC card AI (fig. 8-7 and para 3-74a). The resulting PRST signal is routed to the control circuits on PC card A15.

## 3-32. Receive Interface Circuits

a. All control signals between the CCU and punched tape reader switch between levels of 6 volt and an open kct except for the step data,/acknowledge signal which switches between -6.2 volts and +6.2 volts. These signals are generated by transmitter circuits in the CCU RF1. The receive interface circuits provide an impedance match for the CCU signals, convert them to the punched tape reader logic format ( +4.5 volts active and 0 volt inactive), and restore the sharp turn-on, turnoff required for reliable logic operation in the punched tape reader.
b. The receive interface circuits consist of interface receivers ( E ) through (K) on PC card A4 (fig. 8-9). Interface receivers (E) through (J) provide level shifting and inversion, converting inputs of 0 volt to outputs of +4.5 volts and open circuit input to outputs of 0 volt. Four of the received inputs are active at a low level so that the outputs are active at a high level. These signals are end of message (EOM), end of block (EOB), assigned (ASG), and select (SEL A). A fifth signal (cancel) is received on the RCAN line as a high level when active. After inversion, this results in a low level on not-function cancel line NCAN, indicating a cancel command.
c. interface receiver (K) differs from the other interface receivers in that, although there is level shifting, there is no inversion. Thus, a positive received step 'data acknowledge pulse input (RSDA) results in a corresponding positive output pulse (SDA), whereas a negative receive step data acknowledge pulse results in a nonactive logic level. An inhibit input (SINH) to this receiver is not used and wired to ground.

## 3-33. Advance Control Circuit

a. The advance control circuit generates the advance signal which allows the read cycle control circuit to initiate a new read cycle. The advance function is normally disabled by a stop signal from the stop control portion of the advance control circuit. When any one of four switch-indi-

## Change 2 3-36

cators on control panel A3 is operated, a start pulse is supplied to the stop control to remove the stop condition. This action allows the advance control circuits to generate the advance signal in a way dependent upon the switch-indicator used.
b. For normal operation with the CCU, START switch-indicator $\mathrm{Z7}$ is used. This permits the advance signal to be continuously generated during the header portion of the tape and then generated once for each step/data acknowledge command from the CCU. The remote continuous step control is described in paragraph 339.
c. For the header tape of a two-tape message, PILOT HEADER switch-indicator Z 5 is used. This has the same effect as START switch-indicator Z7 but prevents the generation of an alarm stop signal to the CCU when the tape out condition occurs at the end of the tape. For continuous tape feed under local control, LOCAL TEST switch-indicator Z9 is used. This results in a continuous advance signal. For single-frame operation under local control, SINGLE FEED switchindicator Z6 is used. Each operation of $\mathrm{Z6}$ results in an advance signal which lasts long enough to initiate one read cycle only.

## 3-34. Start Operation

For normal operation of the punched tape reader with the CCU, the advance control circuit is actuated by operation of START switch-indicator Z7 on control panel A3.
a. When START switch-indicator $\mathrm{Z7}$ is operated, this transfers a high level from start closed line STC to start open line STO. The STO signal enables AND gate Z3A on PC card A16 (fig. 821) if the punched tape reader is in a stop condition (stop signal from OR gate Z19B in the stop control circuit is high). The resulting high output of AND gate Z3A sets latch Z7A, Z11A. The high output of this latch activates OR gate Z14B.
b. Prior to activation of Z14B, the high level at the Z14B output clears flip-flop Z17. The low output of OR gate Z 14 B is monitored by AND gate Z 14 A , which is conditioned by the low level at the 1 output of flip-flop Z17 and is enabled by the first negative CLK clock pulse input. Thus, the negative transition produced by Z14A at the trailing edge of the pulse sets flip-flop Z17. The resulting high output of Z17 disables Z14A, preventing Z14A from being enabled by the next CLK clock pulse. The effect is that a single positive pulse is generated by Z14A.
c. The positive pulse produced by AND gate Z14A is supplied to the stop control circuit to remove the stop condition of the punched tape reader by clearing latch Z13.
d. The high output of latch Z7A, Z11A also sets latch Z15 which, in turn, supplies a high level from the Z15B output to clear local test latch Z23, thereby removing a local test condition. In addition, the low level at the Z15A output conditions AND gates Z16A and Z16B. As long as the punched tape reader has not yet been selected by the CCU, the SEL A line from the receive interface circuit is low. This conditions AND gate Z16B. Finally, since the punched tape reader now is not in a stop condition, the stop signal from OR gate Z19A in the stop control circuits is low. This enables AND gate Z16B to produce a high level on line DSG. The DSG line activates a lamp driver on PC card A3 to energize the green indicator in START switch-indicator Z7.
$e$. The white indicator is not energized until the punched tape reader is selected by the CCU. At that time, the SEL A line goes high. This disables AND gate Z16B and is inverted to a low level by inverter Z12B to condition AND gate Z16A. If the punched tape reader is in ready state, OR gate Z8A in the ready control circuit supplies a low level to enable AND gate Z16A.
f. While the punched tape reader is still feeding header tape, the advance signal for the read cycle control circuit is controlled by remote continuous step line RCS which is high until the beginning of the message is reached. The RCS line activates OR gate Z12A to supply a low level to condition AND gate Z2OA. The other input to Z20A is the stop signal from the stop control circuit which goes low as soon as the start pulse is supplied to the stop control circuit. Thus, Z20A produces a low level on not advance line NADV to the read cycle control circuit.
g. When the beginning of the message is reached, the RCS line goes low. However, if the punched tape reader is selected by the CCU, the SEL A line to AND gate $\mathrm{Z4B}$ is high. Each step.' data acknowledge signal received from the CCU results in a positive pulse on the SDA line from the receive interface circuits which enables AND gates Z4B. Thus, Z4B produces a positive pulse on gated step line GS. This pulse is coupled through OR gate ZSB to activate OR gate Z12A. The resulting low level conditions AND gate Z20A to generate the

NADV signal. Thus, each SDA pulse results in a corresponding NADV pulse.
h. Normally, the start condition of the punched tape reader remains until the operator operates STOP switchindicator Z8 on the control panel. When Z8 is operated, the stop control circuit generates a stop signal at the end of a read cycle of the output of OR gate Z19B which clears latch Z15, extinguishing the light in the switchindicator. The stop signal also disables AND gate Z20A, forcing the NADV signal to go high.

## 3-35. Pilot Header Operation

The PILOT HEADER switch-indicator (Z5) on control panel A3 is used to remove the stop condition in the stop control circuits for the header tape of a message consisting of two tapes. When this is done, the punched tape reader operates $\mathrm{Z8}$ is now operated, the stop control circuit produces a low level at the Z13A output of latch Z13. This action enables AND gate Z18A to supply a high level to OR gate Z19A. In addition, if the punched tape reader is deassigned, the pilot header condition can be removed by operating RESET switch S1 on logic assembly Al. This results in a high level on the R8T line to OR gate Z19A.

## 3-36. Local Test Operation

When continuous tape feed under local control is desired, LOCAL TEST switch-indicator Z9 on control panel A3 is used to activate the advance control circuit.
a. When LOCAL TEST switch-indicator $\mathrm{Z9}$ is operated, a high level is switched to local test open line LTO from local test closed line LTC, conditioning AND gate Z3B on PC card A16 (fig. 8-21). This gate also monitors the stop (STP) and not assigned (NASG) signals. Both of these signals are high if the punched tape reader is in a stop condition and has not been assigned by the CCU. The resulting high output of Z3B sets latch Z7B, Z1iB.
b. The high output of this latch activates OR gate Z14B, resulting in a pulse from AND gate ZI4A the same way as for start operation and pilot header operation. This pulse is fed to the .top control circuit to remove the stop condition.
c. In addition, the high output of Z7B, Z11B sets latch Z23 to produce a high level on local test line LT. This signal activates a lamp driver on PC card A3 to energize the filament in LOCAL TEST switch-indicator Z9. The LT signal also ac
tivates OR gate Z12A to cause the generation of a not advance (NADV) signal the same way as the single feed operation. Normally, the NADV signal remains low until STOP switch-indicator Z8 is operated. When Z8 is operated, the stop control circuit generates a stop signal at the output of OR gate Z19B which clears latch Z23, thereby removing the local test condition.

## 3-37. Single Feed Operation

For single frame feed of the tape under manual control, SINGLIE FEED switch-indicator Z6 on control panel A3 is used to activate the advance control circuit.
a. When SINGLE FEED switch-indicator $\mathrm{Z6}$ is operated, a high level ( 4.5 volts dc) is transferred to single feed open line SFO from single feed closed line SFC, conditioning AND gate Z2A on PC card A16 (fig. 8-21. Since this AND gate monitors stop signal STP, it is inhibited unless the punched tape reader is in a stop condition. When Z2A is enabled, the high output sets the latch formed by OR gates Z6A and ZIOA which removes the effects of switch bounce from the signal. The resulting high level output conditions AND gate Z5A and also activates OR gates Z9B and Z14B.
b. The action described in a above results in a single start pulse from AND gate Z14A to latch Z13 to remove the stop condition in the stop control circuit. The start pulse also sets flip-flop Z1 through AND gate Z5A. The resulting high output of $\mathrm{Z1}$ on single feed line SF lights SINGLE FEED switch-indicator Z6 by activating a lamp driver on FC card A3.
c. Single feed signal SF also enables AND gate Z4A unless the punched tape reader has been assigned by the CCU. In this case, the assigned line ASG is inverted to a low level by inverter Z21A to disable AND gate Z4A. This prevents automatic advance of a character position under control of the SINGLE FEED switchindicator; however, tape can still advance under control of the step data acknowledge interface signal SDA from the CCU, gated through AND gate Z4B.
d. When not assigned to the CCU, AND gate Z4A produces a high level when SINGIE FEED switchindicator Z6 is operated. If assigned, AND gate Z4B produce a high level when step data acknowledge signal

SDA is received from the CCU. These signals are routed through OR gate Z8B to OR gate Z12A which feeds a low level to AND gate Z20A. If the other conditioning input to Z2OA is low, a low level is produced on not advance line NADV and routed to the read cycle control circuit on PC card A16.
e. Normally, the NADV signal remains low until the end of the read cycle. At that time the stop line goes high and disables AND gate Z2OA. This line also clears single feed flip-flop Z1A, disabling AND gate Z4A. Thus, another read cycle is not initiated until SINGLE FEED switch-indicator Z 6 is operated again. Even if switchindicator Z 6 is held in the depressed state so that latch Z6A, Z10A remains set, AND gate Z5A does not set flipflop Z1 again. This is because flip-flop Z17 is not cleared until SINGLE FEED switchindicator Z6 is released. At that time, the L4.5volt level is switched back to the SFC line, clearing latch Z6A, ZIOA and, in turn, deactivating OR gate Z14B. The high output of Z14B then clears flipflop Z17. (See para. 3-38f.)

## 3-38. Stop Control

The stop control portion of the advance control circuits generates a stop command for each condition in which it is required to stop the advance control circuit. Normally, the stop command is removed by a start pulse from the advance control circuit when one of the four advance switchindicators on the control panel is operated (PILOT HEADER (Z5), SINGLE FEED (Z6) START (Z7), or LOCAL TEST (Z9)). In the case of SINGLE FEED switch-indicator $\mathrm{Z6}$, the stop command is renewed during the first read cycle. In the case of the other three switchindicators, the stop command is not normally renewed until STOP switch-indicator Z8 is operated. However, a stop command is automatically generated in case of a tape out, alarm stop, or an operator's alarm condition. A stop command is also generated at initial power turn-on and when RESET switch S1 on logic assembly Al is operated.
a. The stop command is generated by OR gate A19B on PC card A16 (fig. 8-21)] Whenever the output of Z19B goes high, AND gate Z20A in the advance control circuit is disabled, thereby preventing a new read cycle from being initiated. The Z19B output is also passed through buffer amplifier Z20B to the STP line. This activates a lamp driver on PC card A3 which energizes STOP switch-indicator Z6 on control panel A3.
b. If the alarm circuits on PC card A15 detect an alarm stop condition, a stop command is produced. The alarm stop condition is indicated by a low level on not alarm stop line NAST. This signal is routed to the interface circuits for transmission to the CCU and is also inverted to a high level by inverter Z24B to activate OR gate Z19B.

The NAST signal is generated by OR gate Z16B on PC card A15 (fig. 8-20). This QR gate is activated by a high level when the cancel control circuit detects a cancel command from the CCU and places a high level on cancel line DCAN. In addition, OR gate Z16B is activated when OR gate Z23A produces a high level output. This is caused by a high level from AND gate Z20A in case of a tape out condition in the middle of message but not in the header tape, by a high level on invalid character line DINC in case an invalid character is detected, and by a high level on tape motion failure line DTMF in case the tape speed is too fast or too slow.
c. If the tight tape alarm circuit on PC card A15 detects a tight tape condition, a low level is produced on not operator's alarm line NOA. This signal is routed to the interface circuits for transmission to the CCU and is also inverted to a high level by inverter Z22B on PC card A16. The high output of Z22B activates OR gate Z19B to cause a stop command.
d. The third input to OR gate Z19B causes a stop command only after a read cycle, which may be in progress, has been completed. Thus, AND gate Z22A supplies a high level output only when the CYCL signal from the read cycle control circuit on PC card A14 is low. The stop conditions which control the other input to Z22A are controlled by latch Z13.
e. One of the ways to initiate a stop command through latch Z13 is to operate STOP switch-indicator Z8 on the control panel. The normally open switch contacts then place a high level on stop open line STPO. This is filtered by resistors R14 and R13 and capacitor C3. The high level sets latch Z13, resulting in a low enabling level for AND gate Z22A and a high level at the output of Z19B at the time the CYCL signal from PC card A14 is low.
f. Automatic generation of a stop command after initiation of a read cycle by SINGLE FEED switchindicator Z6 is controlled by AND gate Z5B. This AND gate is conditioned by a high level which appears on line SF from single feed
flip-flop Z1 at the start of the read cycle. At the count of 30 (read cycle time of 3016), tape motion set line TMS from PC card A14 goes high, enabling Z5B. The resulting high output is passed through OR gate Z9A to set latch Z13.
g. If a tape out condition occurs at any time, even though this may not result in an alarm stop condition (when not operating with the CCU or in the header tape), it does result in a stop command. This is controlled by set operator stop line SOS to OR gate Z9A. A high level is received on the SOS line from OR gate Z7B on PC card A15 whenever a low not out of tape signal NOT is received from the reader mechanism. This signal is inverted to a high level by inverter Z15A to activate OR gate Z7B.
h. The SOS line is also activated when power is first turned on to the punched tape reader and when RESET switch S1 on the logic assembly is operated in the not assigned mode. Power on reset results in a high level on line PRST to OR gate Z11B; operation of RESET switch S1 results in a ground connection on line RSTO to enable AND gate Z15B if assigned line ASG is low. In either case, a high level is received at the output of Z11B to activate OR gate Z7B, placing a high level on the SOS line.

## 3-39. Remote Continuous Step Control

The remote continuous step control circuit allows automatic continuous stepping of the leader portion of the tape when the punched tape reader is under remote (CCU) control.
a. The remote control step (RCS) signal for the advance control circuits is generated by flipflop Z10 on PC card A15 (fig. 8-2d). This flipflop is initially set when power is first turned on to the punched tape reader. Thus, a high level on reset line RST is coupled through OR gate Z6B to the continuous step line (CSTP) which sets Z10. The resulting high level on the RCS line to the advance control circuit ensures that continuous stepping is permitted to begin immediately when one of the two remote advance switchindicators (START or PILOT HEADER) is operated. At the same time, the high level on the RCS line is fed to the data strobe decoder on PC card A14 to disable generation of data strobes. In addition, latch Z26 is cleared by a 9.6 -kc clock pulse from the oscillator (OSC) on PC card A1. Thus, a low level is placed on remote continuous step reset line RCSR. This is fed to PC card A14 to permit initiation of read cycles.
b. Although characters are read from the tape, no data strobes are generated until the first nonidle character is read. Thus, AND gate Z17A monitors idle character line IDC. This line goes high when any one of seven idle characters is being read. Thus, if this line is low during the read cycle, the character being read is not an idle character. The status of the IDC line is checked early in the read cycle to allow time for generation of a data strobe if the line proves to be low. Thus, AND gate Z17A is strobe by not remote continuous step strobe NRSS from PC card A14. The NRSS signal is a negative pulse which is generated once each read cycle at the count of 3 (read cycle time 208). The third input to Z17A (NRCS) prevents enabling of this AND gate unless the punched tape reader is in remote continuous step operation.
c. When the first nonidle character is detected, AND gate Z17A is enabled to pass the negative NRSS pulse at the count of 3 (time 312) in the read cycle. This conditions AND gate Z21A for this duration (104 ,sec). The negative step which appears on oscillator line OSC at the end of this time to advance the timing counter to the next count also enables AND gate Z21A, unless the detected character is an N. The positive step at Z21A output sets latch Z26, thereby placing a high level on line RCSR. This clears flip-flop Z10 so that the RCS line goes low. Thus, data strobe generation at the count of 21 (time 2030) in the read cycle is permitted. Latch Z26 is immediately reset at the count of 4 (read cycle time 416) by the next positive transition on the OSC line.
d. If the first detected character happens to be an N, AND gate 21 does not become enabled because of the high level which appears on the N line. Separate control is used to terminate the remote continuous step mode in this case ( g below).
e. Normally, flip-flop Z10 remains set until the end of the message after which the tape is again presumed to be leader tape until a new nonidle character is detected. The end of message is detected by AND gate Z2B which is conditioned by the SEL A line when the punched tape reader is selected by the CCU. After the last block in the message, both the EOB (end of block) and EOM (end of message) lines are simultaneously activated by pulses from the CCU. Thus, AND gate Z2B becomes enabled to pass a positive pulse through buffer amplifier Z6A to flip-flop Z10. The flip-flop is clocked to the set state by the
negative transition which occurs at the end of the positive pulse.
$f$. If the message does not proceed to a normal end of message conclusion, but is canceled, a cancel signal on the DCAN line from the cancel control circuit is passed through OR gate Z6B to set flip-flop Z10. Also, if a tape out condition occurs with the punched tape reader not in the pilot header mode, AND gate Z19B is enabled to produce a high level which is passed through OR gate Z6B to set flip-flop Z10. It is assumed that the first portion of the next tape will be leader tape unless the first tape was the header tape of a two-tape message (pilot header mode).
g. As described in e above, flip-flop Z10 is set when simultaneous EOM and EOB signals are received from the CCU. The EOM signal indicates that the CCU has decoded an end of message sequence from the tape message. This end of limit sequence consists of two carriage return (CR) characters, eight line feed (LF) characters, and four or more N's. The EOM signal is generated by the CCU as soon as the complete end of message sequence is detected. However, since subsequent N's do not indicate the start of a new message, AND gate Z2ZA does not respond to N's as described in $d$ above. However, if one or more idle characters appear after the last N in a message, the next N is considered the start of a new message. This is determined with the aid of latch Z 5 as described in h and i below.
h. Each decoded N character results in a high level on the N line to inverter Z 13 B . The resulting low output of Z13B is strobed at the count of 3 (time 208) in the read cycle by the negative NRSS pulse to AND gate Z17B. The third input to Z17B is the low level supplied by flip-flop Z10 as long as the punched tape reader is in the remote continuous step mode. This occurs at the beginning of a new tape or after the fourth N in an end of message sequence. The resulting low output of Z17B enables Z21B to set latch Z26 if a low level is received from latch $Z 5$. As soon as the EOM pulse from the CCU is detected, latch Z 5 is set by the high output of buffer amplifier Z6A, thereby disabling AND gate Z21B. Thus, subsequent N's have no effect on Z21B.
i. To condition AND gate Z21B, the sequence of N's must be interrupted by one or more idle characters. These are detected by AND gate Z9A which monitors idle character line IDC. This line is strobed at the count of three in the read cycle by the positive pulse produced by inverter Z13A from the negative NRSS pulse input. The third input to Z9A is the RCS line which
prevents Z9A from being enabled until the end of message has been detected and the punched' tape reader has returned to the remote continuous stepping mode. If an idle character is then detected, AND gate $Z$ 9A clears latch Z5B to provide a low conditioning level for Z21B. Thus, the first N after one or more idle characters causes latch Z26 to be set, thereby terminating the remote continuous step mode. To insure that latch Z5 is cleared in case the message is not ended with a conventional end of message sequence, the CSTP line is also fed to the clear side of the latch. This line goes high at power turn-on, operation of RESET switch S1, cancel, or a tape condition (nonpilot header).

## 3-40. Ready Control Circuit

The ready control circuit generates the ready signal for the CCU unless the punched tape reader is in the local test mode, the remote continuous step mode, or a stop condition.
a. The ready signal is controlled by OR gate Z8A on PC card A16 (fig. 8-21). This OR gate becomes activated if any of the following three conditions exist
(1) The stop condition as indicated by a high level from stop control OR gate Z19B.
(2) The local test mode as indicated by local test signal LT from local test latch Z23.
(3) The remote continuous step mode as indicated by a high level on the RCS line from PC card A15.
b. When none of the inputs to OR gate Z8A is high, a low output is produced. This is inverted to a high level on RDY line by inverter Z24A. The RDY output is fed to the transmit interface circuits for transmission to the CCU.

## 3-41. ITA-2 to ASCII Converter, Block Diagram (fig. 3-21)

a. ITA-2 Decoding. To convert the 58 characters encoded in five ITA-2 data bits into the equivalent characters encoded in eight ASCII data bits, it is first necessary to decode each of the 58 ITA-2 character codes. This is accomplished as follows:
(1) First, the characters represented by the five ITA-2 bits are converted to a two-digit octal
code. The first three bits of the ITA-2 code (designated 11, 12, and 14) specify the least significant digit of the octal code. These three bits are converted to their octal equivalent ( 0 through 7) by a binary to octal converter which identifies the rows in an 8 by 8 matrix (table 3-1). The last two bits of the ITA-2 code (designated 18 and I16 1) are used in specifying the most significant (digit of the octal code. This digit identifies the columns in the 8 by 8 matrix.
(2) Any character in the 8 by 8 matrix is defined by the intersection of the row and column. Thus, the row and column select signals from row and column binary to octal converters are decoded by a decode matrix which activates 1 of 64 output lines depending on the intersection of row and column.
(3) The 8 by 8 matrix in table 3-1 consists of two halves with the characters in columns 0 through 3 being figures characters and those in columns 4 through 7 being letters characters as defined by the ITA-2 code. The shift between letters and figures is determined by the LET and FIG characters. These characters appear in both the letters and figures halves of the matrix When a letters code is detected, a letters-figures register is set to the letters position. This activates a simulated sixth bit (132) to the column binary to octal converter. The sixth bit is necessary since three binary bits are needed to specify the eight octal digits. Alternately, when a figures code is detected, the letters-figures register is set to the figures position and the 132 is deactivated.

(4) Besides the letters and figures codes (LET and FIG), four other codes appear in both halves of the matrix. These are the CR, NUL, LF \& SP codes. Since a total of six codes appears twice, there is a total of only 58 different characters which can be detected.
b. ASCII Encoding. Once the 58 ITA-2 characters are decoded onto 58 separate lines, the
conversion to an eight-bit ASCII code can be performed. This is done as follows:
(1) First, the 58 characters are encoded as two octal digits represented by eight lines each. The two octal digits (designated F and G) for each character can be represented by the ASCII matrix in table 3-1


Table 3-2. ASCII MATRIX. Change 6-42
(2) The circuit which converts the 58 separate lines to the octal row and column code is called an encode matrix. This circuit activates a different combination of a column line and a row line for each of the 58 characters.
(3) Once the conversion to octal coding is complete, the two-digit octal code is converted into its ASCII equivalent by encoding each octal digit into the binary codes specified in figure $3-3$. The parity bit is made active or inactive, as necessary, to make the total sum odd.
(4) The final conversion into ASCII is
made by an octal to binary converter. This circuit converts each row selected into a three-bit binary code which represents the first three bits of the ASCII code. The next four bits are determined by the octal column selection. However, more than eight combinations of these four ASCII bits are needed. Therefore, the octal to ASCII conversion must make allowance for six of the characters which are in two extra columns. These are shown in able 3-2, in columns labeled A and B. The columns are defined by the combination of binary bits which specify them.


Figure 3-21. ITA-2 to ASCII converter, block diagram.

## 3-42. Column Binary-to-Octal Converter

a. The column binary-to-octal converter decodes the states of the two most significant ITA2 bits (I8 and 116) and the letters/figures bit (I32) to activate one of eight different output lines corresponding to each of the eight possible combinations of the three bits. The eight output lines select the eight columns in the 8 by 8 matrix. Each octal column value is equivalent to the binary value of the three input bits.
b. The 18 and $I 16$ bits are amplified and converted to complementary form by inverters Z10A, * Z11B, Z11A, and Z10B on PC card A8 (fig. 813). These bits and the complementary 32 (letters) and 32 (figures) bits for the letters/figures register are then applied in eight different combinations to eight decoder AND gates. The decoding is similar to that for the row binary-to-octal converter. Thus, for octal column 5, the +8, I16, and 32 lines are monitored by AND gate Z14B. These lines are all low when the code for the I8, I16, I32 bits is 101.

## 3-43. Row Binary-to-Octal Converter

The row binary-to-octal converter decodes the states of the three least significant ITA-2 bits (I1, I2, and I4) to activate one of eight different output lines for each of the eight possible combinations of the three bits. The eight output lines select the eight rows in the 8 by 8 matrix. Each octal row value is the equivalent of the binary value of the ITA-2 bits.
a. The three least significant ITA-2 bits (I1, I2, and 14) are initially amplified and inverted by inverters Z20A, Z24A, and Z28A on PC card A8 (fig. 8-13). The resulting not-function bits are inverted again by inverters Z20B, Z24B, and Z28B to provide the true-function of each bit. The complementary bit signals are applied in Fight different combinations to eight decoder AND gates. Only one of the eight AND gates is enabled at any time, depending on the combination of input. data bit levels. Thus, if all three data bits are 0's, the true-function (l1, 12, and 14) at the outputs of inverters Z20B, Z24B, and Z28B are low, thereby enabling AND gate Z15P to place a low level on line_00. This selects row 0 . When data bits 11,12 , and 14 are 1,0 , and 0 , respectively, AND gate Z15A is enabled to place a low level on line 01 since this gate monitors the not-function of the 11 bit (I1) from inverter 19-15/NAVSHIPS 0967-324-0056/TO 31W42G.61 Z20A and the true-functions (12 and 14) of the other two.
b. The other AND gates operate in a similar manner, each gate monitoring a combination of the binary bits corresponding to the binary value of the octal row selection. Thus, for row 5, the binary value is 101. Therefore, AND gate Z23A which controls line 05 becomes enabled when the states of binary bits 11, 12 , and 14 are 1,0 , and 1 , respectively. At that time all inputs to Z23A are low and a low output occurs on line 05.

## 3-44. Letters/Figures Register

a. The letters/figures register generates an I32 bit for the column binary-to-octal converter. This is done by monitoring the decoded letters and figures characters from the matrix decoder. Each figures character switches the register to a 0 for the 132 bit. This condition remains until the next decoded letters character which switches the register to 1 for the I32.
b. The matrix decoder operates from a six-bit code, one bit of which is the 32 bit which is determined by the letters/figures character. Thus, the coding for the letters/figures character is contained in only five bits. Since there are only 32 possible combinations of five bits, the five-bit code of the letters character may activate either of two possible decoder matrix outputs, depending on the previous state of the letters/figures register. However, either of these two lines represents a valid letters character and must be used to set the letters/figures register to the letters state. Alternately, the five-bit code of the figures character may activate one of two possible matrix outputs, either of which must be used to set the letters/figures register to the figures state.
c. The two letters decoder matrix output lines (LTR A and LTR B) are monitored by OR gate Z4A on PC card A7 (fig. 8-12).: When either line is activated, Z4A produces a low output on the LTR C line. Similarly, when either the FIG A or FIG B decoder matrix output is activated, OR gate Z4B produces a low level on the FIG C line.
d. The LTR C and FIG C lines are routed to PC card A\& (fig. 8-13) where they are gated with letters.figures strobe LFS line from PC card A14. The LFS line goes low for each character being read. When the character is a figures character, AND) gate $Z 7 R$ is enabled by low levels at both the LFS and FIG C inputs. Thus Z7B sets
latch Z 6 to place a high level on line $\overline{32}$ and a low level on line 32. The latch remains in this state until a letters character is read. This enables AND gate Z7A to set the latch to the alternate state, placing a high level on line 32 and low level on line 132 .

## 3-45. Decode Matrix

a. The decode matrix decodes the two octal digits from the row and column binary-to-octal converters onto 64 output lines representing the 64 characters specified by the 64 possible combinations of the two octal digits table 3-1). The matrix consists (,f 64 (decoder AND gates, each of which monitors a different combination of the two octal digit,. The 64 decoder AND gates are located on identical PC cards A9 and All (figs.8-14 and 8-16)
b. PC card All contains 32 AND gates which decode the characters in the first four columns of the matrix and PC card A9 contains 32 AND gates which decode the characters in the last four columns of the matrix.
c. The AND gate, which receives a low level at both it. rows select and column select inputs, is enabled to produce a high level output representing the selected character All other AND gates specifying the other 63 characters are inhibited since any row-column combination can satisfy only one AND gate at a time.
d. For example, if the character T is punched on the tape, the binary-to-octal converters activate column 6 and row 0 of the matrix as shown in table 3-1. Thus COLUMN 6 and ROW 0 inputs to PC card A9 are both low The only AND gate which monitors both these lines is AND gate Z17A on PC card A9. Therefore, only Z17A is enabled to produce a high output

## 3-46. Encode Matrix

a. The encode matrix encodes the 64 characters from the decode matrix into two octal digits representing the row and column of the 8 by 8 portion of the ASCII matrix (table 3-2). The encode matrix consists of a set of OR gates located on identical PC cards A10 and A12 tigs. 8-15 and 8-17).
b. Each of the 64 characters (except those in row 0 and column 0 ) is routed to two OR gates, one defines the column digit of the output octal code and the other defines the row digit (table 3-3). The OR gates controlling columns G0, G1, G2, and G3 of table 3-3 are located on PC card A10, and the OR gates controlling
columns G4, G5, G6, and G7 are located on PC card A12,
c. In addition, OR gates are provided for each of rows F1 through F7 on both cards A10 and A12. The respective row outputs are wired together external to the two cards. For example, the output of row 1 OR gate Z11 on PC card A12 is wired to the output of row 1 OR gate Z11 on PC card A01. Thus, if either A10Z11 or A12Z11 is activated, a high output is produced on the common row FI output line to the octal-to-ASCII converter. No OR gate is used for row F0 since this row is assumed to be active whenever the other rows are inactive.
d. As an example of encode matrix operation, assume that the character T is punched on the tape. As indicated in table 3-3 this character is defined by the intersection of row F4 and column G2 in the encode matrix. Thus, the line representing this character is routed to OR gate Z2B on P1 card A10 which controls the line representing column G2 and to OR gate Z14B which controls the line representing row F4. The high level, on the character T line causes both Z2B and Z14B produce high outputs.

## 3-47. Octal-to-ASCII Converter

The row and column octal digits from the encode matrix are converted into the corresponding eight-bit ASCII code by the octal-to-ASCII converter. The eight ASCII bits consist of seven bits ( 1 through 7 ), which define the characters, and one parity bit.

## 3-48. Generation of ASCII Bits 1, 2, 4, 8, 16, 32, and 64

a. ASCII data bits 1,2 , and 4 are defined by rows 0 through 7 of the encode matrix. The signals identifying the seven rows (F1 through F7) are coupled through buffer amplifiers on PC card A13 (fig. 8-18) to three expanded OR gates which convert the octal row selection digit into the equivalent three-bit binary code on ASCII data bit lines 1, 2, and 4. These lines correspond to the binary value of data bits 1,2 , and 3 respectively Each row selection digit (F0 through F7) is encoded by feeding it to the OR gates which control the binary equivalent
lines. For example, F6 converts to 110 (binary 6) on data bit lines 4, 2, and 1 of the ASCII output. When none of the seven row select digits is activated, a row FO
selection is indicated. In this case, all the three binary output lines remain low (000).

| $\begin{gathered} \text { Kows } \\ (\mathbb{F}) \end{gathered}$ |  |  |  | (6) |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | 0 | 1 | 2 | 3 | 4 | 5 | 1. | 7 |
|  | $\begin{aligned} & \text { DATA } \\ & \text { BITS } \end{aligned}$ |  |  | \% | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
|  |  |  |  | 22 | 0 | 0 | 0 | 0 | i | 1 | 1 | 1 |
|  |  |  |  | -16 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
|  | 4 | 2 | 1 | 8 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 |  |  | H | P | x | SP | 1 | 0 | 8 |
| 1 | 0 | 0 | 1 |  | A | I | Q | Y | ! | 1 | 1 | 9 |
| 2 | 0 | 1 | 0 |  | B | J | R | z | - |  | 2 | : |
| 3 | 0 | 1 | 1 |  | C | K | S |  | \# |  | 3 | ; |
| 4 | 1 | 0 | 0 |  | D | L | T |  | \% | - | 4 |  |
| 5 | 1 | 0 | 1 |  | E | M | U |  |  | - | 5 |  |
| 8 | 1 | 1 | 0 |  | F | N | v |  | \& | - | 6 |  |
| 7 | 1 | 1 | 1 |  | G | 0 | W |  |  | 1 | 7 | ! |

## Table 3-3. Encode Matrix

b. ASCII data bits 8, 16, 32, and 64 are defined by columns G0 through G7 of the matrix. Thus, the column selection from the encoder matrix is converted into the equivalent four-bit binary code as specified by table 3-3. This is accomplished by feeding the column G0 through G7 lines to four sets of expanded OR gates on PC card A13 which control data bits 8, 16, 32 , and 64 and then modifying the results with additional gating to compensate for the special characters in columns $A$ and $B$ of the ASCII matrix in table 3-2.

## 3-49. Generation of ASCII Parity Bit

a. The parity bit is developed by determining whether the sum of the other seven data bits is odd or even. This determination is made in two stages. First, a determination as to whether the sum of data bits 1,2 , and 4 is odd or even and as to whether the sum of data bits $8,16,32$, and 64 is odd or even. Then, these two sums are compared to determine if the total sum is odd or even.
b. There are four possible combinations of data bits 1, 2, and 4 involving an odd sum (001, 010, 100, and 111). These combinations are represented by the octal row select digits FI, F2, F4, and F7. Thus, if the character read from the tape is in rows F1, F2, F4, and F7 of the ASCII matrix, the sum of data bits 1,2 , and 4 is odd. This condition is detected by routing the row F1, F2, F4, and F7 lines to expanded OR gate Z5A, Z17A on. PC card A13 (fig. 8-18). If any of the lines are high, the OR output is low, indicating an odd sum.
c. The parity detection for data bits $8,16,32$, and 64 is performed in a similar manner. Thus, the combinations of these bits involving an odd sum is represented by column select digits G0, G3, G4, and G7. If the character read from the tape involves an even sum
of data bits $8,16,32$, and 64 , a high level is applied to expanded OR gate Z5B, Z17B and a low level output is produced.
d. The odd and even sum outputs for the two sets of data bits are fed to the comparator circuit formed by AND gates Z2A and Z6A, and OR gate Z7B for final parity evaluation. Thus, AND gate Z2A receives both high inputs only if both the bit 1, 2, 4 sum is even and the bit $8,16,32,64$ sum is even and AND gate Z6A receives both low inputs only if the two sums are odd. In either case, a high output activates OR gate Z7B to result in a low level which is inverted by AND gate Z11A. The resulting high level on the parity bit line (128) keeps the total bit sum odd.

## 3-50. Timing Generator

The timing generator controls the timing sequence for each read cycle. The read cycle lasts for 64 counts of a $104-\mu \mathrm{sec}$ oscillator period ( 6.66 ms ) for high speed operation of the punched tape reader and 512 count $(53.4 \mathrm{~ms})$ for low speed operation. The timing generator consists of three circuits: a read cycle control circuit which starts the cycle on receipt of an advance signal; the timing counter and its associated decoders which control the length of the read cycle and the events which occur during it by generating a series of time sequenced pulses; and a cycle complete control which terminates the read cycle after 64 counts or 512 counts of the 104$\mu \mathrm{sec}$ increment. The circuits of the timing generator are described in paragraphs 3-51 through 3-62.

## 3-51. Read Cycle Control

The read cycle control allows the timing counter to begin counting 9.6 -kc clock pulses ( $104-\mu \mathrm{sec}$ period) from an oscillator on PC card AI when an advance command is received from the advance control circuit. Normally, counting is permitted to continue until the cycle complete control detects the end of the read cycle ( 64 counts or 512 counts, depending on the mode).
a. The advance command is received in the form of a low level on not advance line NADV at AND gate Z9B on PC card A14. This conditions Z9B to become enabled by negative $9.6-\mathrm{kc}$ OSC pulses from the oscillator. A second conditioning input for Z9B is provided by remote continuous step reset line RCSR. This line is low as long as the message part of the tape is being read. Thus, the first negative OSC pulse after the NADV line goes low results in a positive pulse at the output Z9B, setting read cycle latch Z13. This starts the read cycle interval and places a high level on line CYCL. The latch also supplies a low conditioning level to AND gate Z9A in the timing counter circuit to permit counting operation.
b. The read cycle normally continues until a cycle complete signal is received on line CC from the cycle complete control. The high level on line CC is passed through OR gate Z1A to clear latch Z13.
c. To insure that no read cycle occurs if the portion of the tape passing through the read head is not the message portion, when a high level occurs or. line RCSR, the signal is passed through OR gate Z1A to clear latch Z13.
d. Latch Z 13 is also cleared when power is first turned on to the equipment and .when RESET switch indicator S 1 on logic assembly Al is operated. In either case, a high level is applied to OR gate Z1A on reset line RST.

## 3-52. Timing Counter

The timing counter is a binary counter which goes through a 64-count sequence for each read cycle in high speed operation and 512-count sequence in low speed operation.
a. The timing counter consists essentially of 10 flip-flops on PC card A14 ffig. 8-19. Prior to the start of a read cycle, a high level is produced by read cycle
control latch Z13 at the Z13A output. This level is directly applied to the clear inputs of the first four counter stages (Z17, Z21, Z25, and Z26). In addition, this level is coupled through buffer amplifier Z19B to counter reset line CRST which clears the remaining counter flip-flops.
b. Counting operation is allowed to begin when the Z13A output goes low at the start of a new read cycle. This conditions AND gate Z9A which is then strobed by successive negative 9.6 -kc pulses on line OSC from the oscillator. Thus, Z9A produces positive pulses at 9.6 ke on count 0 line CO. The first stage of the timing counter (Z17) is clocked at each negative transition of the 9.6 kc clock pulses. The gated set input to Z 17 also receives the 9.6 -kc clock pulses to permit alternating setting of the flip-flop. Alternate clearing of the flip-flop is permitted by a high level on the CYCL line from latch Z13 to the gated clear input to Z17.
c. Each subsequent stage of the timing counter is clocked by the 1 output of the preceding stage. Thus, each stage changes state when the preceding stage is cleared (the 1 output goes low). This satisfies the requirements for conventional binary counter operation. Thus, the successive stages become set for the first time at the counts of $1,2,4,8,16,32,64$, 128, 256, and 512. However, if the punched tape reader is in high speed operation, the high level which appears at the 1 output of flip-flop Z24 when the count of 64 is reached causes the cycle complete control circuit to terminate the read cycle. This causes the Z13A output of read cycle latch Z13 to go high, disabling AND gate Z9A and preventing further clocking of the first counter stage. Also, the Z13A output simultaneously clears all counter stages. Thus, the timing counter is never permitted to exceed the count of 64 in high speed operation.
d. In low speed operation, the cycle complete control circuit does not become activated until the last stage of timing counter (Z18) becomes set at the count of 512 . Thus, a complete 512 -count read cycle is permitted in low speed operation.
$e$. The 1 outputs of the first six counter stages are designated C 1 through C 6 . These outputs go high at the counts of $1,2,4,8,16$, and 32 . The C1 through C6
outputs, as well as the subsequent flip-flop output, are monitored by decoder AND gates to generate signals at specific times in the timing counter time cycle.

## 3-53. Timing Decoder

The timing decoder consists essentially of AND gates on

PC card A14 (fig. 8-19) which decode specific counts in the timing counter to produce sequenced control signals during each read cycle. The decoder functions are described in baragraphs 3-54 through 3-61. The timing relationships explained in these paragraphs are summarized in figure 3-22


Figure 3-22. Timing decoder, overall timing diagram

## 3-54. Decode Inhibit

All of the timing decoder signals are generated during the first 64 counts of the timing counter. Thus, only the first five stages of timing counter (1, 2, 4, 8, 16, 32) are monitored. However, in low speed operation when the count goes up to 512, it is necessary to inhibit the generation of the decoded signals in subsequent count cycles of the first five stages after the count of 64. This is accomplished by AND gates Z14A and Z14B which operate effectively as a single AND gate that monitors the 1 outputs of the last four counter stages $(64,128$, $256,512)$. As long as the count has not yet reached 64, these 1 outputs are all low (the flip-flops are cleared). Thus, the AND gates are enabled and a low level is placed on decode inhibit line DINH. After the count of 64 , one or more of the last four flip-flops is set. Thus, at least one of the inputs to the AND gates is high and a high output is produced on the DINH. This inhibits the other decoder AND gates.

## 3-55. Advance Solenoid Drive

a. The advance solenoid drive pulse for the advance solenoid in the reader mechanism is initiated on the count of 1 and extends up to the count of 18 . To initiate this pulse, AND gate Z15 monitors the I outputs of the counter flip-flops corresponding to the counts of 4,8 , 16, and 32. These lines are all initially low. However, AND gate Z 15 does not become enabled until the count of 1 when the 1 count flip-flop (Z17) is set. The low level at the 0 output of Z17 enables Z15 to produce a high output which sets latch Z4. This places a low level on advance solenoid driver line ASD. Line ASD is connected to solenoid driver SOL DR on PC card AI which sends a high current ground level through advance solenoid line AS. This is the drive pulse line for the drive solenoid in reader mechanism assembly A2[fig. 8-6].
b. To terminate the advance solenoid drive pulse, AND gate Z16B on PC card A14 monitors the 0 outputs of the 2 and 16-count flip-flops (Z21 and Z27). The first time these flip-flops are
set simultaneously is at the count of 18. At that time, Z16B produces a high output on reset advance solenoid driver line RASD which clears latch Z4.
c. The advance solenoid drive pulse is also terminated when a stop command is generated by the stop control circuits. Thus, when a high level is received on stop line STP, OR gate Z19 is activated to clear latch Z4.
d. To insure that latch Z 4 is initially in the clear state when power is first turned on, a high level received on reset line RST from PC card A15 is passed through OR gates Z1A and Z19A to clear latch Z4.

The register reset signal resets the input data register at the beginning of each cycle. This signal is generated as a high level on the count of 1 in the timing counter. This is controlled by AND gate Z8B which monitors count-of-2 line C2 and the output of inverter Z16\& The C2 line goes high for the counts of 2 and 3, 6 and 7, etc. (fig. 3-23). As described for the remote stepping strobe, the Z16 output goes low for the counts of 1 and 3 only. Thus, AND gate Z8B is enabled for the count of 1 and places a high level on line RRST for this count.

## 3-56. Register Reset


Z168

C2

RRST


Figure 3-23. Register reset, timing diagram.

## 3-57. Input Data Sample

a. The input data sample signal is used to gate data into the input data register. This signal is generated as a low level on line IDS from the counts of 16 through 20 for each normal data read cycle. For each read cycle in remote continuous stepping operation, the IDS goes low for the counts of 1 through 20.
b. Operation for normal data read cycles is controlled by AND gates Z11 Band Z7B which function together effectively as a single AND gate that produces a high level at the Z7B when all inputs to both AND gates are low. The two AND gates monitor the 0 output of the count of 16 flip-flop (Z27) and the 1 outputs of the count of 4 and 8 flip-flops. All these lines are low only for the counts of 16 through 19 (fig. 3-24). Thus, Z7B produces
a high output for this duration. The Z7B output is integrated by capacitor C1 and resistor R3 to slow the rise time at the leading edge of the signal. After inversion in OR gate Z7A, the Z7B output results in a negative pulse on the IDS line for the counts of 16 through 19.
c. During remote continuous step operation, AND gate Z8A becomes conditioned by a low level on not remote continuous step line NRCS. During the counts of 1 through 17, the advance solenoid drive line (ASD) is low, enabling Z8A to produce a corresponding high output. This is combined with the Z7B output in OR gate $\mathrm{Z7A}$ to produce a low level on the IDS for the counts of 1 through 19.


Figure 3-24. Input data sample, timing diagram.

## 3-58. Tape Motion Set

The tape motion set signal is used in the alarm circuits for tape motion sensing alarm control. This signal is generated as a high level on line TMS for the counts of 30 and 31 in the timing counter. This is controlled by AND gate Z10A which monitors the inverted reset
advance solenoid driver line (RASD) and the output of AND gate Z12B.
a. The inputs to AND gate $\mathrm{Z12B}$ are the 0 outputs of the 4 and 8 count flip-flops (Z25 and Z26) and the 1 output of the 32 count flip-flop (Z28). Thus, AND gate Z 12 B is enabled for the counts of 12 through 15 and 28 through 31 fig. 3-25.
b. The RASD line is controlled by AND gate Z16B which monitors the 0 outputs of the 2 and 16 count flip-flops. Z21 and Z27) Thus, Z16B is enabled for the counts of 15 and !9, 22 and 23, 26 and 27, and 30 and 31. The resulting high level on line RASD during these counts is inverted to a level by inverter Z10B. Since

Z10B and Z12B produce low levels simultaneously only during the counts of 30 and 31 , AND gate $\mathrm{Z10A}$ is enabled only for these two counts. Thus, a high level is produced on tape motion set line TMS only for the counts of 30 and 31 .


Figure 3-25. Tape motion set, timing diagram.

## 3-59. Not Remote Continuous Step Strobe

a. The remote stepping strobe, which is used to allow the advance control circuits to check idle characters when in the remote continuous step mode. is generated as a low level on line NRSS for the count of 3. in the timing counter. This is controlled by AND gate Z6B which monitors the 0 output of the count-of-2 timing counter flip-flop (Z21) and the output of inverter Z16A.
b. Flip-flop 7 Z 21 is set for the counts of 2 and $3,6 \mathrm{an}(\mathrm{d} 7$, etc. (fig. . $2-2 f 6$ ). Thus, the $\mathrm{Z} 21-0$ line is low for these counts. However, AND gate Z6B also monitors the output of AND gate Z15A after inversion by inverter

Z16A. As described for the advance solenoid drive decoding, AND gate Z15 monitors the 1 outputs of the flip-flops corresponding to the counts of $4,8,16$, and 32 . Thus, this AND gate is disabled from the count of 4 and on. Up to the count of $4, \mathrm{Z15}$ is enabled only when the count-of-I flip-flop (Z17) is set. This occurs for the counts of 1 and 3 . Thus, $Z!5$ produces a high level and Z16A, in turn, produces a low. level for these two counts. Thus, AND gate Z6B is enabled for the count of 3 only and produces a low level on line NRSS for this count.


Figure 3-26. Remote stepping strobe, timing diagram.

## 3-60. Tape Motion Strobe

The tape motion strobe is used in tape motion alarm generation by the alarm circuits. This signal is generated as a low level on line NTMS for the counts of 60 through 63 in the timing counter. This is controlled by AND gates Z6A and Z11A which function effectively as a single AND gate. The two AND gates monitor the 0 outputs of the 4 , 8, 16, and 32 count flip-flops (Z25, Z26, Z27, and Z28). Thus, all flip-flops must be set before the AND gates are enabled. This occurs at the count of $60(4+8+16+$ $32=60$ ) and continues until the count of 64 when decode inhibit line DINH inhibits all decoding. Thus, a low level is produced by AND gate Z6A on line NTMS for the counts of 60 through 63.

## 3-61. Data Strobes

a. Data strobes are generated as high levels on line DST for the count of 21 in each read cycle. This is controlled by AND gate Z 20 which monitors the 0 outputs of the 1, 4, and 16 count flip-flops (Z17, Z25, and Z27). Thus, all flip-flops must be set before the AND gate is enabled. This occurs at the count of 21 (1-4 + $16=21$ ). The AND gate also monitors the 1 outputs of the 2 and 8 count flip-flops (Z21 and Z26), both of which are low at the count of 21 .
b. In addition, the 1 output of 32 count flip-flop (Z28) is monitored through AND gate Z12 to prevent the generation of another data strobe at the count of 53 (32 +21 ). Thus, the high level from Z28 disables Z12 from the count of 32 to 64 . From the count of 64 and on, Z20 is disabled by the decode inhibit line (DINH).
c. To prevent the generation of data strobes during the idle characters between messages and at the start of a tape, the high level which appears on remote continuous step line RCS during these portions of the tape disables AND gate Z12A. The high output of Z12A, in turn, disables Z20. In addition, to prevent generation of data strobes when the advance control circuits are in a stop condition, a high level on stop line STP from PC card A16 disables AND gate Z12A.

## 3-62. Cycle Complete Control

In high speed operation, the cycle complete control circuit generates a cycle complete signal when the timing counter has reached a count of 64. In low speed operation, the cycle complete signal is not generated until the timing counter has reached a count of 512 .
a. Selection between high and low speed operation is made by operating HIGH SPEED/LOW SPEED switch-indicator Z3 on the control panel (fig. 8-2). When this push-to-set/push-to-reset device is operated to the low speed state, the common dc return is connected to low speed input line LSI. This low level activates lamp driver Z1B on PC card A3. The resulting ground output lights the LOW SPEED filaments in the switch-indicator.
b. The LSI low level signal is also fed to PC card A14 fig. 8-19) to condition AND gate Z5B. When the count 512 flip-flop (Z18) in the timing counter becomes set, its 0 output places a low level on low speed complete line LSC. This enables Z5B to produce a high output which is routed

Change 6 3-55
through OR gate Z1B to cycle complete line CC. The high output from Z 1 B resets latch Z 13 , which resets all counter stages to 0 and prepares the timing generator for the beginning of a new read cycle.
c. Similarly, when the switch-indicator is operated to the high speed state, the common dc return is connected to high speed input line HSI. This low level activates lamp driver Z2A on PC card A3. The resulting ground output energizes the HIGH SPEED filaments in the switch-indicator. The HSI low level signal also conditions AND gate Z5A on PC card A14. When the count 664 flip-flop (Z2P) in the timing counter is set, its 0 output places a low level on high speed complete line HSC. This enables Z5A to produce a high output which is routed through OR gate Z1B to cycle complete line CC. The high output from Z1B resets latch Z13, which resets all counter stages to 0 and prepares the timing generator for the beginning of a new read cycle.

## 3-63. Data Register

The data register stores the five ITA-2 data bits or eight ASCII bits for each character from the reader mechanism to insure that all data bits are available to the CCU when the data strobe is transmitted.
a. The data bit signals are generated by eight sensing switches (S1 through S8) on reader mechanism assembly A2 (fig. 8-6). These switches control corresponding data bit lines (B1 through BS) to the data register on PC card A7 (fig. 8-12). When no hole is sensed by any switch, a ground connection is made to the corresponding $p$ line. When a hole is sensed by any line, the line goes to a high level ( +4.5 volts) established by a corresponding voltage divider on PC card A7 which is returned to +6.2 volts. The +6.2 volt source is developed by Zener diode VR1 operating from a +12 -volt source.
b. When reading an ASCII $t$ ape, all eight data bit lines represent valid data bits on the tape. When reading an ITA-2 tape, data bit lines B2 through B6 represent the five data bits on the tape for each frame. Data bits $\mathrm{B} 1, \mathrm{~B} 7$, and B 8 are disregarded.
c. Simultaneous storage for data bit signals B1 through B8 is provided by eight latches on PC card A7. All eight latches are placed in the set state at the start of each read cycle. This is accomplished by a high level which appears on register reset line RRST at the count of the 1 in the timing counter. The RRST signal is
passed through OR gate Z 16 B to the set side of the eight latches.
d. The eight data bit signals are gated to the set inputs of the eight latches by corresponding AND gates. For each read cycle, the input AND gates are conditioned for counts of 16 through 19 of the timing counter. This is controlled by the input data sample signal (IDS) from the timing counter. The IDS signal, which is low from the count of 16 through 19, is passed through OR gate Z16A to condition the eight input AND gates. Thus, at the count of 16 the data is passed through the input AND gates, clearing those latches for which a 1 data bit is not received and leaving the others set. The resulting levels at the 1 outputs of the eight latches are routed to the output data gates on PC card A7 for use in ASCII operation. For ITA-2 operation, the five latch outputs for bits B2 through B6 are designated I1, 12, I14, 18, and 116, and are routed to the ITA-2 decoder.

## 3-64. Output Data Gates

The output data gates select either the eight ASCII data bits from the data register or the ITA-2/ASCII converter for transmission to the CCU.
a. The selection between ASCII and ITA-2 operation is made by setting the code select switch S2 on the logic assembly panel to either the ASCII or ITA-2 position. In the ASCII position of the switch, a +4.5 -volt level is connected to ASCII switch line ASW. This enables eight AND gates on PC card A7 fig. 8-12 which monitor the outputs of the eight latches in the data register. These outputs are then passed through output OR gates which control the eight data bit lines to the interface transmitters. The output lines are designated by the binary weight of the data bits (IA, 2A, 4A, 8A, 16A, 32A, 64A, and 128A).
b. When code select switch S 2 is set to ITA-2, a +4.5 -volt level is connected to line ISW which conditions an alternate set of eight AND gates on PC card A7. These gates monitor the eight data bit outputs (1, 2, 4, 8, 16, 32, 64 and 128) of the ITA-2/ASCII converter. The data bits are then fed through the output OR gates to the interface transmitters.

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## 3-65. Character Decoder

a. The character decoder monitors the ASCII output of the output data gates for the occurrence of 13 special characters. One of these is the N character which is used in end of message detection by the remote continuous step control circuit. Another seven are idle characters which are monitored by the idle character detection. One of the special characters (CB) is an invalid character and is monitored by the invalid character detection. The remaining four special characters (BEL, EM, DC4, AT) are not invalid but are also used by the invalid character detector together with some of the idle characters to aid in checking for invalid characters.
b. The 13 special characters are detected by 13 decoder AND gates on PC card A6 (fig. 8-11). Each of these gates monitors a combination of the first seven ASCII bits corresponding to the character being detected. The eighth bit is a parity bit and is not a factor in determining the character. When all seven inputs to any AND gate are low, the AND gate is enabled to place a high level on the corresponding detected character output line. Thus, each AND gate monitors the truefunctions of those bits which are O's for that character and the not-functions of those bits which are 1's for that character. Seven input inverters receive the truefunction input bits from the data register and convert them to not-function form for use as needed.
c. The idle character detector consists of OR gate Z 10 and inverter Z6B. The OR gate monitors seven idle character outputs of the character decoder. When any one of the seven idle characters is detected, the OR gate produces a low output which is inverted to a high level on idle character line IDC by inverter Z6A. This is routed to the remote continuous step control circuit on PC card A15.
d. The invalid character detection is performed by OR gate Z3B which produces a high output on invalid character line INC when an invalid character is detected. One of the invalid characters is the CB character detected by AND gate Z28. When this character is detected, Z28 produces a high output which activates OR gate Z3B.
e. The other two inputs to Z3B are supplied by AND gates Z7B and Z4B which monitors invalid characters involving l's in bits C and 7 and C's in bits 6 and 7 . Thus, if bits 6 and 7 are both 0 's the $32 \mathrm{~A}(6)$ and $64 \mathrm{~A}(7)$ lines to AND gate Z3A are both low. This results in a low output which enables AND gate Z7B unless the character is one of eight special characters which are not
considered invalid even though bits 6 and 7 are 0's. All other characters with O's for bits 6 and 7 are invalid. The eight special characters are detected by OR gates Z 11 and Z12B. When any one of these special characters is detected, Z11 produces a low output which is inverted by inverter Z7A to disable AND gate Z7B. If none of these characters is detected, Z7B produces a high output which activates OR gate Z3B.
f. Similarly, if bits 6 and 7 are both 1's, the N32A and N64A inputs to AND gate Z8B are low, enabling Z8B to produce a low output which enables AND gate Z4B unless a DEL or AT character is detected. These are the only two characters in which l's for bits 6 and 7 are not considered cause for rejection as invalid. When either of these two special characters is detected, Z8A is disabled by a high input and supplies a corresponding high input to disable AND gate Z4B. Otherwise, Z8A supplies a low level to Z4B which becomes enabled to activate OR gate Z3B when both bits 6 and 7 are 1's.

## 3-66. Alarm Circuits

a. Alarm Stop. The alarm stop signal (NAST) is generated as a low level by an alarm stop circuit on PC card A 15 (fig. 8-20). This circuit consists of OR gates Z23A and Z16A which monitor alarm signals from the following separate alarm circuits:
(1) Cancel control circuit (para 3-67).
(2) Tape out alarm circuit (para 3-68).
(3) Tape motion alarm circuit (para 3-69).
(4) Invalid character alarm circuit (para 370).
b. Operator Alarm. The operator alarm signal (NOA) is generated as a low level by the tight alarm circuit (para 3-71) when a tight tape condition is sensed.
c. Audible Alarm Reset. The audible alarm reset signal (AR) is controlled by the audible alarm reset control circuit (para 3-72).

## 3-67. Cancel Control Circuit

a. When a cancel signal is received from the CCU during a data block, Lilt, cancel control circuit causes CANCEL indicator DS2 on the control panel to light.

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b. The cancel signal is detected by AND gate Z 4 A on PC card A15, fig. 8-20). If the cancel signal is received from the CCU during a data block when the select line is active, the receive interface circuits supply low levels on lines NCAN and NSEL. These enable AND gate Z4A which sets latch Z8. The resulting high output of the latch on the DCAN line activates a lamp driver on PC card A3 to energize CANCEL indicator DS2 on control panel A3. Also, alarm stop line NAST goes low and the punched tape reader stops. If tie cancel signal comes at the end of a message, NAST goes low and remote continuous step line RCS goes high. The punched tape reader then steps in the remote continuous step mode to the next nonidle character of the next message or to the end of the tape.

## 3-68. Tape Out Alarm Circuit

The tape out alarm circuit monitors the status of the end of tape sensor switch in reader mechanism assembly A5. If a tape out condition is sensed when a message is in progress and the tape is rot a header tape, an alarm stop is indicated and TAPE OUT indicator DS5 on the control panel is lighted. If the tape reader is not assigned to the CCU, the tape out condition also causes the TAPE OUT indicator to be lighted. However, instead of an alarm stop, a simple nonalarm stop is generated instead.
a. The NC contacts of the end of tape sensor switch on the reader mechanism (fig. 8-6] are held open by the presence of tape in the read station. When the end of the tape is reached, the contacts close and a ground level no tape signal is produced. This is routed to AND gates Z14B, Z19A, and Z19B on PC card A15 (fig. 8-20) on no tape line NOT. If a message is in progress, the AND gate Z14B is enabled to produce a high output which sets latch Z18. The resulting high level at the Z18A latch output is passed through OR gate Z23B to detected tape out line DTO. This line activates lamp driver Z3A on PC card A3 to energize TAPE OUT indicator DS5. At the same time, the low level at the Z18B output of the latch enables AND gate Z20A unless a high level is received on pilot header line PH from the pilot header detector on PC card A16. Thus, unless the punched tape reader is in pilot heads Z20A produces a high output which activates the alarm stop circuit.
b. The detection of an in-message condition is made by latch Z3. When a message is initiated, the first step/data acknowledge signal from the CCU causes a
gated stop pulse (GS) from PC card A16 to set the latch. The resulting low level at the Z3A output conditions AND gate Z14B to accept a no tape indication.
c. The end of a message is identified by simultaneous end of block (EOB) and end of message (EOM) signals from the CCU. The resulting high levels on the EOB and EOM lines enable AND gate Z2B which produces a high level if the select signal from the CCU is still present (SELA is high). The resulting high output from Z2B is coupled through buffer amplifier Z6A and OR gate Z7A to clear latch Z3. If a message is canceled, latch Z 3 is also cleared. In this case, OR gate Z7A receives a high level on the DCAN line from the cancel control circuit. Also, if the punched tape reader becomes deassigned in midmessage, a high level on not assigned line NASG clears latch Z3. In addition, latch Z3 is cleared by a high level to OR gate Z7A on reset line RST when RESET switch S1 on logic assembly A4 is operated and when power is first turned on to the equipment.
d. If the punched tape reader is not assigned to the CCU, a low level on assigned line ASG conditions AND gate Z19A. Thus, if no tape line NOT goes low, Z19A is enabled to produce a high output which activates OR gate Z23B, causing TAPE OUT indicator DS5 to light. The NOT signal is also inverted to a high level by inverter Z15A to activate OR gate Z7B which supplies a stop signal to the stop control circuit on PC card A16.

## 3-69. Tape Motion Alarm Circuit

The tape alarm circuit monitors the tape motion pulses from reader mechanism A2. If these pulses are not received within a specified portion of each read cycle, a tape motion failure signal is generated which initiates an alarm stop and causes MOTION FAIL indicator DS4 on the control panel to light.
a. In the reader mechanism (fig. 8-6), tape motion is sensed by light from a lamp passing through a shutter which is controlled by the tape drive mechanism. The shutter allows light to ,pass once each read cycle. This is sensed by a photocell, and causes the photocell to conduct electricity during the time that the shutter is open in each read cycle. One end of the photocell is
connected to a +12 -volt source of dc and the photocell produces a +1.2 -volt positive pulse once each read cycle. This pulse is amplified by a photocell amplifier on circuit card A2 in the reader mechanism (figs. 4-15) and 8-6 part 2). The photocell amplifier consists of a three stage dc-coupled amplifier, the last stage being an emitter follower. When the photocell is activated, it produces a closed circuit from pins E2 to E3 of amplifier A2, producing the 1.2 -volt dc positive pulse from the +12 volt supply and voltage-dropping resistor R1. The positive pulse is amplified by stages Q1 and Q2, limited by Zener diode limiter D1, and applied through emitter follower Q3 to pin E6 of the amplifier as the output tape motion pulse on the H SIGNAL OUT line.
b. The positive output tape motion pulse produced at the output of the photocell amplifier provides an indication of tape speed since the time from the start of the read cycle to the occurrence of the read pulse increases as the tape slows down and decreases as the tape speeds up. For the purposes of the tape motion alarm circuit, the tape motion pulse is considered satisfactory if it is high after the count of 32 in the timing counter but goes low before the count of 60 .
c. The tape motion pulse is routed on line TM to latch Z27 and inverter Z20B on PC card A15 (fig. 820). Latch Z27 is initially held in the set state during counts 30 and 31 of the timing counter by tape motion set signal TMS from the timing control decoding circuits on PC card A14. If the TM line goes high after this time, the latch is set. However, if the TM line has not gone high when the count of 60 is reached, an alarm is generated. This alarm is controlled by AND gate Z2RB which is conditioned at the count of 60 by a low level on not tape motion strobe line NTMS, from PC card A14. The NTMS line goes low for the counts of 60 through 63. If latch Z27 is still set at the count of 60, AND gate Z28B is enabled to produce a high output which sets latch Z24.
d. When latch Z24 is set, a high level is produced on tape motion failure line DTMF. This high level activates the alarm stop control circuit on PC card A15 and is also routed to PC card A3 to activate lamp driver Z2B. The resulting ground output of Z2B energizes MOTION FAIL indicator DS4 on the control panel.
e. The TM pulse is also inverted by inverter Z20B and is applied as a negative pulse to AND gate Z28A. This AND gate is also conditioned during the counts of 60 through 63 by the NTMS signal. Thus, if the

TM pulse extends into count 60, Z28A is enabled to produce a high output which sets latch Z24.

3-70. Invalid Character Alarm Circuit The invalid character alarm circuit monitors the output of the invalid character detector on PC card A6. To insure that the invalid character indication from the invalid character detector is meaningful, this indication is sampled during data strobe time by AND gate Z2A on PC card A15.

Thus, if invalid character signal INC is high when data strobe pulse DST is generated, AND gate Z2A produces a high output which sets latch Z22. The resulting high level on invalid character line DINC activates the alarm stop circuit and is also routed to lamp driver Z1C on PC card A3. This energizes INVALID CHARACTER indicator DS3 on the control panel.

## 3-71. Tight Tape Alarm Circuit

The tight tape alarm circuit samples the tight tape signal from reader mechanism once each read cycle. If a tight tape condition is present, an operator's alarm is activated and TIGHT TAPE indicator DS6 on the control panel lights. The N.O. contacts of the tight tape sensor switch on the reader mechanism fig. 8-6) are open as long as the tape is not too tight. However, when a tight tape condition occurs, the contacts close. causing a ground level tight tape signal to be sent on line TT to AND gate Z14A on PC card A15. This AND gate is strobed once each read cycle by not remote step strobe NRSS. This signal goes low during the count of 3 at the beginning of each read cycle. If the TT signal is also low, Z14A produces a positive pulse output which sets latch Z12. The resulting high level on line DST activates a lamp driver on PC card A3 to energize TIGHT TAPE indicator DS6 on control panel A3. The DTT signal is also inverted by OR gate Z16A to place a low level on not operator alarm line NOA.

## 3-72. Audible Alarm Reset Control Circuit

If the punched tape reader is assigned by the CCU, the audible alarm reset control circuit generates an audible alarm reset signal (AAR) when AUDIBLE RESET switch Z 1 on the control panel is pressed. This signal is fed through the transmit interface circuits to the CCU to reset
the audible alarm.
a. Closure of the AUDIBLE RESET switch Z 1 contacts transfers a high level to line ARO which is fed to debouncing latch Z25 on PC card A16 (tiq. 8-21) The resulting positive step at the Z25B output of the latch is converted into a sharp positive pulse by differentiator C 1 , R11. The pulse is then coupled through OR gate Z26B which activates line AAR. Positive feedback through capacitor C2 makes the OR gate function as a single shot. The pulse width is determined by the time required to charge up C2 through resistor R12 to a potential at which the feedback voltage is insufficient to keep Z26B activated. At that time, the Z26B output returns to a low level and C2 quickly discharges through diode CR1.
b. To prevent generation of the AAR pulse when the punched tape reader is not assigned by the CCU, a low level on assigned line ASG from the receive interface circuits is inverted to a high level by inverter Z21A. This action prevents Z25 from initiating a step when the pushbutton is pressed.

## 3-73. Transmit Interface Circuits

The ready signal from the ready control circuit is shifted from the punched tape reader switching levels ( 0 volt and +4.5 volts) to CCU interface switching levels ( +6.2 volts and 0 volt) by the transmit interface circuits. This permits the CCU to send the select signal through the receive interface circuits. When the select signal is present, the eight output ASCII data bits and the data strobe are gated through the transmit interface circuits to the CCU.
a. Ready Signal. The ready signal from the ready control circuit on PC card A16 is inverted to an active level of 0 volt and an inactive level of +6.2 volts by transmitter (A) on PC card A4 (fig. 8-9) The resulting transmit ready (TRDY) output is sent to the CCU.
b. Data Strobe. The data strobe (DST) from the data strobe control circuits on PC card A14 is gated into transmitter (J) on PC card AS by the SEL B select line from the receive interface circuits (fig. 8-10). When the select input from the CCU is active, the SEL B line is high and the positive DST strobe pulses are accepted and converted to polar pulses (TDST) to the CCU, switching from +6.2 volts to -6.2 volts.
c. ASCII Outputs. The eight output ASCII data bits (DB1 through DB8) from the input register are gated into transmitters (A) through (H) on PC card A5 by
the select line from the receive interface circuits. The SEL A select input is buffered by OR gates Z1A and Z1B to condition the eight transmitters. When the CCU has selected the punched tape reader, a high level on each input bit line results in a +6.2 -volt output. A low level on each input line results in a -6.2-volt output.
d. Alarm Stop and Operator Alarm Signal. The not alarm stop (NAST) and not operator alarm (NOA) signals from the alarm logic controls circuits on PC card A1S are applied to transmitters (B) and (C), respectively, on PC card A4 (fig. 8-9). The resulting transmit TAST and TOA outputs are at +6.2 volts when an alarm condition exists and at 0 volt when no alarm condition exists.
e. Audible Alarm Reset Signal. The audible alarm reset signal (AAR) from the alarm control circuits is fed to transmitter (D) on PC card A4. When the punched tape reader is assigned to the CCU, the ASG line from the receive interface circuit goes high. This conditions transmitter ( D ) to produce an open circuit on line TAAR to the CCU, resetting the audible alarm in the CCU. If either input goes low, the TAAR output goes to 0 volt.

## 3-74. Detailed Operation of Discrete Circuits on PC card A1 (fig. 8-7)

a. Power On Reset Circuit. The power on reset circuit produces a power on reset pulse when power is turned on. Power turn-on results in the $+4.5-$ volt dc supply level being coupled through resistor R3 to the circuit output. However, at the same time, the 48 -volt supply current gradually charges up capacitor C1 through resistor R2. As the voltage at the junction of C1 and R2 reaches approximately -11.5 volts, voltage dropping Zener diode VR1 starts to conduct, allowing the output voltage to drop below +4.5 volts. As the charge continues to build up, the output voltage continues to drop until it reaches 0 volt. The output is prevented from going below this value by diode CR1.
b. Solenoid Drivers. Solenoid driver Q1, Q2, Q3 is activated by a 0 -volt input to resistor R5. This results in a negative voltage at the junction of voltage divider R5, R6 to drive transistor Q1 into conduction. Conduction of Q1 causes a 0 -volt level at the Q1

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collector, which supplies base current for Q2. This allows transistor Q2 to go into conduction s, that a -12volt level is coupled through resistor R10 to drive transistor Q3 into conduction. The Q3 collector is connected through the external solenoid winding to the 48 -volt supply. Thus, the solenoid draws current from the -48 -volt return line (ground) through Q3. If the input to the solenoid driver goes to +4.5 volts, all operations are reversed and Q3 is cut off so that the solenoid is deenergized. Capacitor C2 slows down the rise and fall times of the Q3 output and diode CR3 sets the bias for the base of Q3 at +0.7 volt when Q2 is cut off. Solenoid driver Q4, Q5, Q6 operates in a similar manner.
c. Oscillator Circuit. The oscillator circuit produces $9.6-\mathrm{kc}$ clock pulses. When power is turned on, current flows from the +12 -volt power source through resistor R18, diode CR6, potentiometer R20, and resistor R19 to charge capacitor C5. The output voltage from the oscillator is +4.5 volts at this time, as determined by the voltage regulator circuit consisting of Zener diode VR2, resistor R18, and filter capacitor C4. The 9 -volt output of the voltage regulator is applied to voltage divider R22, R23 to produce the +4.5 -volt output. When the voltage across C5 is sufficient to fire unijunction transistor Q7, the charging current is bypassed through Q7 and resistor R21. The resulting positive voltage across R21 drives transistor Q8 into conduction, thereby causing the output of the circuit to fall to 0 volt. After capacitor C5 has discharged through the emitter of Q7, the current into the emitter of Q7 is insufficient to maintain conduction. Thus, Q7 goes into cutoff. The resulting 0 volt output across R21 causes Q8 to go into cutoff. Thus, the output voltage returns to 4.5 volts. Capacitor C5 now begins charging again as described above. The cycle repeats indefinitely as long as power is present. The repetition rate is determined by the time required to charge capacitor C5. This is adjusted by potentiometer R20.

## 3-75. Detailed Operation of Discrete Circuit Logic Elements

The detailed circuit operation of discrete circuit logic elements is described in paragraphs 3-76 and 3-77. The component makeup of each type of logic element is shown in figures 3-27 through 3-32. However, since one example of each type is shown in these figures, refer to table 3-4 for a detailed listing of the corresponding components in the logic element of each type.

## 3-76. Detailed Operation of Discrete Circuit Logic Elements on PC Card A4

a. Type RCVR-LA Interface Receiver (fig. 327). The RCVR-1A receiver converts a 0 -volt input from the CCU to +4.5 volts and an open circuit input from CCU to 0 volt. When the transmitting source becomes an open circuit, the input signal becomes +6.2 volts. This signal is coupled by resistor R25 and bias network R27, and Zener diode VR4 to the base of transistor Q8, driving Q8 into conduction. This action results in a 0 -volt output at the Q8 collector. When the input signal goes to 0 volt, transistor Q1 is cut off and a +4.5 -volt output is coupled through resistor R28 to the load.
b. Type RCVR-1B Interface Receiver (fig. 328). The type RCVR-1B receiver operates in the same way as the RCVR-1A (a above), except coupling is accomplished by constant voltage drop diode CR3, and resistor R13.
c. Type RCVR-2 Interface Receive(fig. 3-29). The type RCVR-2 interface receiver converts a +6.2 -volt input from the CCU to +4.5 volts and a -6.2 -volt input to 0 volt. A +6.2 -volt input causes transistor Q10 of differential amplifier composed of Q10 and Q11 to go into conduction and causes transistor Q11 to go into cutoff. The negative voltage at the collector of Q10 is coupled through resistor R38 to drive transistor Q12 into cutoff. Thus, the output assumes the +4.5 -volt level supplied through resistor R41. If, however, the input to the circuit is -6.2 volts, the base of Q10 assumes a negative potential established through resistors R33 and R34. Thus, Q10 is driven into cutoff and Q11 into conduction. The positive level at the collector of Q10 drives Q12 into conduction so that the output goes to 0 volt.
d. Type XMTR-1A Interface Transmitter (fig. 330). Inputs from the punched tape reader logic circuits switching between 0 volt and +4.5 volts are coupled through impedance matching network R1, R2, R3 to the base of inverter Q1. When the input is 0 volt, Q1 is cut off and supplies an open circuit to the CCU which provides a connection through a load resistor to +6.2 volts. When the input is +4.5 volts, Q1 is driven into conduction, resulting in a 0 -volt output to the CCU.
e. Type XMTR-1B Interface Transmitter (fig.

3-31). The type XMTR-1B transmitter operates in the same way as the XMTR-1A transmitter described in d above, except diodes CR1 and CR2 are added to provide an AND function for two input signals, both of which must be +4.5 volts to produce the 0 output.



Figure 3-28. Type RCVR-1B interface receiver, schematic diagram.

Figure 3-27. Type RCVR-1A interface receiver, schematic diagram.


Figure 3-29. RCVR-1C interface receiver, schematic diagram.
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Figure 3-30. Type XMTR-1A interface transmitter, schematic diagram.


Figure 3-31. Type XMTR-1B interface transmitter, schematic diagram.

Table 3-4. Discrete Circuit Logic Element Components

| $\underset{\text { card }}{\text { PC }}$ | Logic element type | Logic element reference designation | Component reference designation |
| :---: | :---: | :---: | :---: |
| A4 | XMTR-1A | (A) | R1 R2 R3 Q1 |
|  |  | (B) | R4 R5 R6 Q2 |
|  |  | (C) | R7 R8 R9 Q3 |
|  | XMTR-1B | (D) | R10 R11 R12 CR1 CR2 Q4 |
|  | RCVR-1A | (E) | R13 R14 R15 R16 CR3 Q5 VR1 |
|  |  | (F) | R17 R18 R19 R20 CR4 Q6 VR1 |
|  |  | (G) | R21 R22 R23 R24 CR5 Q7 VR3 |
|  | RCVR-1B | (H) | R25 R26 R27 R28 Q8 VR4 |
|  |  | (J) | R29 R30 R31 R32 Q9 VR5 |
|  | RCVR-1C | (K) | R33 R34 R35 R36 R37 R38 R39 R40 R41 CR6 Q10 Q11 Q12 |
| AS | XMTR-2 | (A) | R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 C1 Q1 Q2 Q3 Q4 CR1 CR2 |
|  |  | (B) | R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 C2 Q5 Q6 Q7 Q8 CR3 CR4 |
|  |  | (C) | R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 C3 Q9 Q10 Q11 Q12 CR5 CR6 |
|  |  | (D) | R31 R32 R33 R34 R35 R36 R37 R38 R39 R40 C4 Q13 Q14 Q15 Q16 CR7 CR8 |
|  |  | (E) | R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 C5 Q17 Q18 Q19 Q20 CR9 CR10 |
|  |  | (F) | R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 C6 Q21 Q22 Q23 Q24 CR11 CR12 |
|  |  | (G) | R61 R62 R63 R64 R65 R66 R67 R68 R69 R70 C7 Q25 Q26 Q27 Q28 CR13 CR14 |
|  |  | (H) | R71 R72 R73 R74 R75 R76 R77 R78 R79 R80 C8 Q29 Q30 Q31 Q32 CR15 CR16 |
|  |  | (J) | R81 R82 R83 R84 R85 R86 R87 R88 R89 R90 C9 Q33 Q34 Q35 Q36 CR17 CR18 |

## 3-77. Detailed Operation of Discrete Circuit Logic Elements on PC Card A5

a. The type XMTR-2 interface transmitter on PC card A5 (fiq. 3-32) receives card reader inputs switching between 0 and +4.5 volts de at AND gate diodes CR1 and CR2. When both inputs are +4.5 volts, the diodes are cut off and bias network R1, R2, R3 drives transistor Q1 into conduction. Loading for Q1 is provided by resistors R4 and R5. The low voltage at the junction of R4 and R5 turns on transistor Q2 to result in a
positive level at the Q2 collector. This drives transistor Q3 into conduction and transistor Q4 into cutoff. Thus, the +6.2 -volt supply voltage is drawn through (43and resistor R 8 to the circuit output.
b. When a 0 -volt level is applied to either input diode CR1 or CR2, bias network R1, R2, R3 allows Ql to go into cutoff. The resulting positive output of Q1 drives Q2 into cutoff so that a negative voltage appears at the Q2 collector. This voltage drives q 3 into cutoff and , 4 into conduction. Thus, the -6.2 -volt supply is drawn through Q4 and resistor R9 to the circuit output.


Figure 3-32. Type XMTR-2 interface transmitter, schematic diagram.

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## Section IV. GENERAL FUNCTIONING OF TRANSMISSION IDENTIFICATION GENERATOR

## 3-78. Transmission Identification Generator, Block Diagram

 (fig. 3-33)The transmission identification generator (TIG), when installed in the punched tape reader and used with the CCU, provides the automatic generation of a transmission identification (TI) character sequence. The TI sequence precedes the first data character of each message read and transmitted by the punched tape
reader to the CCU. The T1 characters generated by the TIG are a programmable sequence of ASCII alphabetic, numeric, and machine function characters as defined in paragraph 3-84. Processing of the data generated by the TIG is performed by electronic circuits located both in the punched tape reader logic assembly and in the TIG assembly and by manual switches located on the TIG control panel. These functions are described in baragraphs 3-79 through 3-84


Figure 3-33. Transmission identification generator, block diagram.
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## 3-79. Interface with Punched Tape Reader (fig. 3-34)

Punched tape readers having a TIG installed modifies punched tape reader operation during generation of the TI character sequence. Figure 3-34 provides a timing diagram showing transfer of both Tl sequence characters to the CCU and transfer of punched tape data read by the punched tape reader.
a. Data interface lines between the punched tape reader and the CCU are gated through data multiplex circuits in the TIG. During the TI generation at the start of each message, the data multiplex circuitry will inhibit data being read from the punched tape and enable transmission of TIG generated special characters, channel designation characters, and numerical message sequence characters.
b. The SELECT line from the CCU and the DATA STROBE line to the CCU are gated through the TIG control circuitry. These interface control lines are inhibited between the punched tape reader and the CCU during the generation of the TI sequence. At the start of each message, these signals are used by the TIG to control the transfer of TI sequence characters. During TI sequence generation, the TIG control circuitry will enable gating of one character on the ASCII data lines to the CCU, each time a positive step data acknowledge pulse is received from the CCU providing the select line is high and the TIG has completed its previous character. The data character is then accompanied by a TIG generated positive data strobe pulse. After the completion of the TI sequence, the TIG control circuitry will then enable transfer of these signals between the punched tape reader and the CCU, and the punched tape reader will then transfer data characters in the normal manner.
c. Other interface with the punched tape reader includes the 9.6 KC clock signal to provide timing functions for the TIG circuitry. NCRS, NAST, and PRST signals enable reseting of TIG circuitry upon power turnon, detection of end of message, cancel, and alarm stop conditions.

## 3-80. End of Medium

The last character of the TI sequence is the end of medium (EM) character. The ASCII coding of EM character is generated by the CCU in response to an active level on the EM interface line thus, during generation of the EM level, the TIG will place a NUL character on the ASCII data lines. The EM character signifies to the CCU and to the AUTODIN message
switch that a short block (less than 80 characters) is being transmitted (TM 11-7440-214-15).

## 3-81. Message Sequence Function

The message sequence counter maintains a record of the number of messages transmitted. This counter is incremented by each paper tape message transmitted by the terminal having the TI sequence included. A visual display of the next message sequence number is provided on the TIG front panel. Manual controls on the front panel enable presetting of the message sequence counter to any number from 000 to 999 . The counter multiplex enables transmission of the count in the message sequence counter as a part of the TI sequence by gating only one of three numerical characters at a time to the data selection circuits.

## 3-82. Dual TIG Installations

At terminals having dual punched tape readers, dual TIG assemblies may be installed. In this case, interface between the two TIG units consist of advance counter pulses. Thus, regardless which punched tape reader, TIG unit transmits the message, the message sequence counters in both TIG assemblies are incremented by one.

## NOTE

To initially obtain the same count in both sequence counters, manually set both counters to the same number. Once the counters are set, they will then remain in step.

## 3-83. Off-Line Function

An OFF-LINE/ON-LINE switch is contended on the TIG control panel. When you have the TIG in the off-line mode, data transfer between the punched tape reader and the CCU is functionally the same as operation in units without a TIG installed. In the off-line mode, the TIG functions only to enable gating of the punched tape reader/ CCU interface lines. In the on-line mode, the TI sequence is generated at the beginning of each message.

## 3-84. Signaling Code

a. Data Signal Code. The signaling code used for all data transfer between the punched tape reader and the TIG and between the TIG and


Figure 3-34. Punched tape reader/TIG, timing diagram
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the CCU is eight-bit ASCII code. Refer to the signaling code chart[fig. 3-3). Seven of the ASCII bits contain the data. The eighth is the parity bit which is high or low, as necessary, to have odd parity for the transmitted character.
b. Transmission Identification Format. The TIG will generate a transmission identification (TI) format to precede each message transmitted from the punched tape reader. The TI format provides for a channel designator sequence, a channel sequence number, ASCII machine function control characters SI, SO, CR, and LF, and the ASCII character NUL. The TI sequence consists of thirteen to sixteen ASCII characters formated for transmission as follows:

| Position NR | 123 | 4 | 567 | 8 | 91011 | 12 | 1314 | 15 | 16 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Character | Z C Z | C | A B C | S | 123 | S | $\begin{array}{ll} \mathrm{C} & \mathrm{C} \\ \mathrm{R} & \mathrm{R} \end{array}$ | L | N U L |

(1) Positions 1, 2, and 3. The function of the "ZCZ" characters is to identify ACP-127 start of message. A stran)ing capability, to be accomplished at time of TIG installation, is provided on the PC card you install in the A1A2 (or A4A2) logic assembly. This strapping enables optional transmission or nontransmission of the part or all of the three characters. Thus, the T1 format may begin with position $1,2,3$, or 4 .
(2) Position 4. The function of the "C" character is to identify a modified ACP-127 start of message sequence.
(3) Positions 5, 6, and 7. Three alphabetical characters are placed in these positions to identify the channel designator for your particular terminal location. A strapping capability to be accomplished at time of TIG installation is provided on the PC card you install in the AA2 (or A4A2) logic assembly. This strapping enables generation of any ASCII character in each of the three positions.
(4) Position 8. The shift out (SO) control character is used for machine control.
(5) Positions 9, 10, and 11. One numeric character from 0 to 9 is placed in each position. These characters identify the channel sequence number of the message to be transmitted. The message number placed in these positions is the number displayed on the TIG front panel at the start of message transmission.
(6) Positions 12, 13, 14, and 15. Shift in (S1), two carriage returns (CR), and one line feed (LF) character are placed in these positions for machine control.
(7) Position 16. The null (NUL) character (all lines except parity have a low level) is required for proper operation of the CCU when the end of medium (EM) line is activated by the TIG.

## 3-85. Logic Diagrams

a. The data processing and control functions of the transmission identification generator are performed by logic circuits on two printed circuit (PC) cards. One of these you will find located in the punched tape reader logic basket A1A2 or A4A2 locations and the other is fastened to the TIG front panel. Thus, the electrical operation of each PC card is represented in chapter 8 by a logic diagram rather than a conventional schematic diagram. The logic diagrams show all input and output connections of the card including power connections but do not show the circuit components which make up the individual logic elements. Basic descriptions of the logic elements are given in baragraphs 3-88 and 3-90.
b. One of the logic elements in the transmission identification generator is made of discrete circuit components. The schematic representation and a description of the circuit operation for this type of logic element is given in paragraph 3-92

## 3-86. Logic Signal Notation

a. In general, logic signals in the transmission identification generator switch between a high level of + 4.5 volts and a low level of 0 volt. Some signal lines are considered activated when the level is high whereas others are considered activated when the level is low. The state indicators (small circles) at the input and outputs of logic elements indicate which lines are activated by a high level (state indicator absent) and which lines are activated by a low level (state indicator present).
b. All significant logic signals are assigned a functional name. Many of the functional names are also assigned mnemonic designations. To permit the active state of a signal to be identified by its functional name or mnemonic designation, the high level is arbitrarily designated true or logic 1 for signal naming purposes, whereas the low level is arbitrarily designated not-true or 0 logic 0 . Thus, the signal is a true-function if it is
active on a high level and a not-function if it is active on a low level. Not-function signals are prefixed by the Letter N (for example: NSELECT:not selected). Refer to the following chart for identification of mnemonic
designations used in the TIG modification to the punched tape reader.

| TIG logic signals-mnemonics and functional names |  |  |  |
| :---: | :---: | :---: | :---: |
| Mnemonic | Functional name | Mnemonic | Functional name |
| CTR $2^{\circ}$ | COUNTER BIT $2^{\circ} 2^{1}, 2^{2}$, and $2^{3}$ ). | NROM A1 | NOT READ ONLY MEMORY BIT A1 (A2). |
| DST | DATA STROBE | NSELECT | NOT SELECT |
| EM | END OF MEDIUM | PRST | POWER ON RESET |
| LED $\mathrm{V}_{\mathrm{cc}}$ | ISOLATOR-MCD2 (LIGHT EMMITTING DIODE) VOLTAGE. | SDA | STEP DATA ACKNOWLEDGE |
| NAST | NOT ALARM STOP | SELA | SELEC'i A |
| NEMPULSE | NOT END OF MEDIUM PULSE. | TIGDST | TIG DATA STROBE |
| NOFFLINE | NOT OFF-LINE | TIGSELA | TIG SELECT A |
| NINTIG | NOT INCREMENT OTHER <br> TIG COUNTER. | TIG 1A | TIG DATA BIT 1 A (2A, A4, through 128A). |
| NRCS | NOT REMOTE CONTINUOUS STEP. |  | DATA BIT 1A (2A, 4A, through 128). |

c. In the functional descriptions, the terms high and low are used for +4.5 -volt and 0 -volt levels. Pulses or steps going from 0 volt to +4.5 volts are called positive pulses or steps and those going from +4.5 volts to 0 volt are called negative pulses or steps.

## 3-87. Logic Diagram Symbol Notation

a. Typical integrated circuits and discrete circuit logic elements are shown in figure 8-21.2. Inputs and outputs of integrated circuit logic elements are identified by the wire terminal numbers of the integrated circuit modules in which the elements are located.
b. Two tagging lines are used within each logic symbol for identification purposes.
(1) The first tagging line in each symbol identifies the logic element type. The various types of integrated circuits and discrete circuit logic elements are described in baragraphs 3-88 through 3-92
(2) The second tagging line in each logic symbol identifies the reference designation of the logic element. This reference designation must be preceded by the PC card reference designation to form the complete designation of the logic element.

## 3-88. Integrated Circuit Modules

a. The integrated circuit modules used in the TIG are of several types as described in the following paragraphs. Reference designations for the integrated circuit modules are $\mathrm{Z} 1, \mathrm{Z2}, \mathrm{Z} 3$, etc.
b. Some of the integrated circuit modules contain only one logic element, whereas others contain
two or more. In those cases where two or more logic elements are contained in one integrated circuit module and the elements are shown separately on the logic diagram, you will find designations A, B, C, and D; for example Z1A, Z1B, etc.
c. Power supply inputs to the individual logic elements are not shown on the logic diagrams, however, discussion on the individual circuits identifies power pins. In addition, you will find a chart on each logic diagram in chapter 8, identifying the power inputs to the various modules.

## 3-89. Operation of Individual Integrated Circuit Modules

The operation of the individual integrated circuit modules used in the TIG is described below. Logic symbols are given for each type of module, using typical tagging lines. Since some of the modules are classified as medium scale integration (MSI), functional block diagrams are also illustrated in those cases.
a. Type 7402 Module. Four two-input type 7402 gates are located on each type 7402 module (fig.335). These may be either inverting AND gates for low inputs (case A) or inverting OR gates for high inputs (case B), by tying both inputs together, type 7402 gates may also function as inverters (case C). Terminal 14 of type 7402 module is connected to +Vcc and ground is applied to terminal 7.
b. Type 7410 Module. Three-input type 7410


Figure 3-35. Type 7402 module, logic symbols.
gates are located on each type 7410 module (fig. 3-36). These may be either inverting AND gates for high inputs (case A) or inverting OR gates for low inputs (case B). Terminal 14 of the type 7410 module is connected to +Vcc and ground is applied to terminal 7.


TM 7440-219-15-119
Figure 3-36. Type 7410 module, logic symbols.
c. Type FF-7474 Module. Two type 7474 flipflops are located on each type FF-7474 module (fig. 337).
(1) The flip-flops can be set either by a
low level at the $S$ input or by a high level at the D input which is clocked by a positive step on the clock (CLK) input. The flip-flops can be cleared by either a low level on the C input or by a low level on the D input which is clocked by a positive step on the CLK input.
(2) Open circuits on the S, C, or D inputs are equivalent to a high level. The type 7474 flip-flop module receives power inputs of +Vcc on terminal 14 and ground on terminal 7 .


TM 7440-219-15-120
Figure 3-37. Type FF-7474 module, logic symbols.
d. Type MLPX-74151 Module. One data selector, multiplexer circuit is contained in each type MLPX-74151 module (A, fig. 3-38). This circuit will select one of eight data sources as the data output. A functional block diagram of the circuit is provided for your analysis of circuit operation (B) fig. 3-38).
(1) A low level must be applied to the E (enable) input. When this occurs, one of the eight data inputs (Do through D,-) is gated through to output $Y$ and W depending upon the binary value of the three data select inputs (20, 2', and 22). Output $Y$ will have the same value as the selected data input line and output VW will develop an inverted level. The following truth table shows output levels for each of the input combinations:

| Inputs |  |  |  |  |  |  |  |  |  |  |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $2{ }^{2}$ | $2^{1}$ | $2^{0}$ | E | D | $\mathrm{D}_{1}$ | $\mathrm{D}_{2}$ | $\mathrm{D}_{1}$ | D. | D ${ }_{\text {s }}$ | $\mathrm{D}_{8}$ | $\mathrm{D}_{\text {\% }}$ | Y | w |
| X | X | X | 1 | X | X | X | X | X | X | X | X | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | X | X | X | X | X | X | X | 1 | 0 |
| 0 | 0 | 1 | 0 | X | 0 | X | X | X | X | X | X | 0 | 1 |
| 0 | 0 | 1 | 0 | X | 1 | X | X | X | X | X | X | 1 | 0 |
| 0 | 1 | 0 | 0 | X | X | 0 | X | X | X | X | X | 0 | 1 |
| 0 | 1 | 0 | 0 | X | X | 1 | X | X | X | X | X | 1 | 0 |
| 0 | 1 | 1 | 0 | X | X | X | 0 | X | X | X | X | 0 | 1 |

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A


TM 7440-219-|5-12|

| Outputs |  |
| :---: | :---: |
| $\mathbf{y}$ | $\mathbf{w}$ |
| $\mathbf{1}$ | 0 |
| 0 | 1 |
| $\mathbf{1}$ | 0 |
| 0 | 1 |
| 1 | 0 |
| 0 | 1 |
| 1 | 0 |
| 0 | 1 |
| 1 | 0 |

Figure 3-38. Type MLPX-74151 module, logic symbol and functional diagram.
(2) Power inputs consist of + Vcc applied to terminal 16 and ground connected to terminal 8.
e. Type MLPX-74153 Module. Two data selector/multiplexer circuits are contained in each type MLPX-74153 module (A, fig. 3-39). Each circuit will select one of four data sources and gate a single data line output. A functional block diagram of the circuit is provided for analysis of circuit operation (B, fig. 3-39). Power inputs consist of + Vcc applied to pin 16 and ground applied to pin 8 . Common address lines ( $2^{0}$ and $2^{1}$ ) are used to select one of four input data lines to each circuit within the module. However, selection of one of the four data input lines $\left(1 D_{0}\right.$ through $1 D_{3}$, or $2 D_{0}$ through $2 D_{3}$ ) is individually controlled through a separate enable line ( 1 E or 2 E ) to each circuit. Look at the following truth table to determine output level for the various input combinations:
f. Type BDC CTR-74160 Module. One fourbit binary coded decimal (BCD) counter is located on each type BCD CTR-74160 module (A, fig. 3-40). This counter can be either reset to all low outputs or preset to provide a binary output equivalent to any decimal number 0 through 9 . When clocked, this counter will count from 0 through 9 and back to 0 . A carry output is provided at a count of 9 . A functional block diagram

| Address |  | Inputs |  |  |  |  | Output | Inputs |  |  |  |  | Output |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $2^{1}$ | $2^{0}$ | 1 E | 1D. | $1 \mathrm{D}_{1}$ | $1 \mathrm{D}_{3}$ | 10, | 1 Y | 2 E | 2D. | $2^{\text {D }}$ | $2 \mathrm{D}_{2}$ | 2 D, | 2 Y |
| $\mathbf{X}$ | $\mathbf{X}$ | 1 | X | X | X | X | 0 | 1 | X | X | X | X | 0 |
| 0 | 0 | 0 | 0 | X | X | X | 0 | 0 | 0 | X | $\overline{\mathrm{X}}$ | X | 0 |
| 0 | 0 | 0 | 1 | X | X | X | 1 | 0 | 1 | X | X | X | 1 |
| 0 | 1 | 0 | X | 0 | X | X | 0 | 0 | X | 0 | X | X | 0 |
| 0 | 1 | 0 | X | 1 | $\mathbf{X}$ | X | 1 | 0 | X | 1 | X | X | 1 |
| 1 | 0 | 0 | X | X | 0 | X | 0 | 0 | X | X | 0 | X | 0 |
| 1 | 0 | 0 | X | $\mathbf{X}$ | 1 | X | 1 | 0 | X | X | 1 | X | 1 |
| 1 | 1 | 0 | X | X | X | 0 | 0 | 0 | X | X | X | 0 | 0 |
| 1 | 1 | 0 | X | $\mathbf{X}$ | $\mathbf{X}$ | 1 | 1 | 0 | X | X | X | 1 | 1 |



A


Figure 3-39. Type MLPX-74153 module, logic symbol and functional diagram.
(1) Power inputs consist of + Vcc applied to pin 16 and ground applied to pin 8. BCD outputs from the counter (QA through QD) are provided on pins 11 through 14 with the QA output being the least significant bit.
(2) The reset (RST) input to the module is asynchronous and a negative step on the RST input will reset all four flip-flops causing the QA and Q,, outputs to go low. The counter then is inhibited from counting until the RST input goes to a high level. Refer to timing diagram or figure 3-41
(3) Presetting of the counter requires two conditions; a low level on the LOAD input and


Figure 3-40. Type BCD CTR-7416;0 module, logic symbol and functional diagram.
a positive step on the clock (CLK) input. When this occurs, the $Q_{A}$ through $Q_{A}$ outputs will as-
sume the level provided on the $2^{0}$ through $2^{3}$ data input lines. This is illustrated on the timing diagram (fig. 341) by showing presetting of the counter to the value of $7 \mathrm{Q}_{\mathrm{D}}$ through $Q_{A}=0111$ respectively). The value of 7 is arbitrarily selected, thus note that counter may be set to
the binary equivalent of any decimal value 0 through 9 .
(4) The two E (enable) inputs must have a high level applied to enable counting. See timing chart on figure 3-41 which shows that a low on either E input will

## ILLUSTRATED BELOW IS THE FOLLOWING SEQUENCE:

1. CLEAR OUTPUTS TO ZERO.
2. PRESET TO BCD SEVEN.
3. COUNT TO EIGHT, NINE, ZERO, ONE, TWO, AND THREE.
4. INHIBIT


Figure 3-41. Type BCD CTR-74160 module, timing diagram.
inhibit counting. Also note that the carry (CRY) output develops a high level when the counter outputs $Q_{A}$ through $Q_{D}$ equal a binary equivalent of 9 . If the CRY output of one type BCD CTR74160 module is connected to the E inputs of a second module, stepping of the second module would then be inhibited except for every 10th clock pulse.
g. Type PAR GEN-74180 Module. One eight-bit input parity generator is located on each type PAR GEN74180 module providing both even and odd parity output capability (A, fig. 3-42). A functional block diagram of the circuit is provided in B figure 3-42.
(1) Levels are applied to module pins 3 (even) and 4 (odd) to determine the state of the complimentary
sum odd and sum even outputs. As utilized in this equipment, a low enable level is applied to odd input and a high inhibit level is placed on the even input.
(2) Data bit inputs are applied to the 1 through 7 inputs. Module circuitry will make a comparison of the sum of high level inputs and develop a level on the two output pins as indicated in the following truth table:

| Inputs |  |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: |
| SUM of 1's at |  |  | SUM | SUM |
| 1 through 7 | EVEN | ODD | EVEN | ODD |
| ODD --------------- | 1 | 0 | 1 | 0 |
| EVEN -------------- | 1 | 0 | 0 | 1 |



B
TM 7440-219-15-125
Figure 3-42. Type PAR GEN-74180 module, logic symbol and functional diagram.
(3) Power inputs to module are applied to terminals $14\left(\mathrm{~V}_{\mathrm{CC}}\right)$ and 7 (ground).
h. Type REG-74195 Module. One four-bit register is located on each type REG-74195 module. The register will operate in two modes; shift (in direction $Q_{A}$ toward $Q_{D}$ ) and parallel (broad-side) load. The two modes are illustrated in A and B, figure 3-43 and a functional block diagram is provided for understanding of the operation in C, figure 3-43.
(1) The clear (CLR) input line must remain at a high level during loading and shifting of the register. Referring to the functional block diagram, note that a low level on the CLR input will reset the four flip-flops to a cleared state.
(2) In the case A configuration, loading of the $Q_{A}$ flip-flop and shifting of all four flip-flops is accomplished synchronously when the shift/load (S/L) input is high and a positive step occurs on the clock (CLK) line. After each shift,


Figure 3-43. Type REG-74195 module, logic symbols and functional diagram.

Q, flip-flop assumes the state indicated in the following truth table as determined by the level on the J and K inputs:

| Inputs <br> at $t_{n}$ |  | Output at $t_{n+1}$ | Notes |
| :---: | :---: | :---: | :---: |
| J | K | $\mathrm{Q}_{\mathrm{A}}$ | $\mathrm{H}=$ high level |
| L | H | No change |  |
| L | L | L | $\mathrm{L}=$ low level <br> $\mathrm{t}_{\mathrm{n}}=$ bit time before <br> clock pulse |
| H | H | H | $\mathrm{t}_{\mathrm{n}+1}=$ bit time after <br> clock pulse |
| H | L | Toggle |  |

(3) In the case B configuration, parallel loading is accomplished by gating four bits of data applied to the $A, B, C$, and $D$ inputs with a negative enable level on the S/L input. Referring to the functional block diagram, note that the next positive step on the CLK line will cause the four flip-flops to assume the state determined by the level on each of the four respective parallel input lines By connecting the $S$, 'L line to ground serial shifting is inhibited.
(4) In both case A and B configurations, $+\mathrm{V}_{\mathrm{Cc}}$ is applied to terminal 16 of the module and ground is connected to terminal 8.
i. Type CONTROL74H87 Module. One 4-bit true/complement/one/zero element with common control lines are contained in the CONTROL74H87 module (A, fig. 344). The functional block diagram for this circuit is illustrated in B, figure 344.
(1) Power inputs consist of $+\mathrm{V}_{\mathrm{Cc}}$ applied to terminal 14 and ground applied to terminal 7.
(2) This circuit will either gate the true levels applied to the four input pins ( $D_{1}$ through $D_{4}$ ) or invert them to compliment form, or set all four outputs ( $\mathrm{Y}_{1}$ through $\mathrm{Y}_{4}$ ) to a low level logical 0 or a high level logical 1 independent of the state of the data inputs.
(3) The following truth table shows module outputs:

| Control inputs |  | Outputs |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $B$ | $C$ | $Y_{1}$ | $Y_{2}$ | $Y_{3}$ | $Y_{4}$ |
| 0 | 0 | $D_{1}$ | $D_{2}$ | $D_{3}$ | $D_{4}$ |
| 0 | 1 | $D_{1}$ | $D_{2}$ | $D_{3}$ | $D_{4}$ |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 |

j. Type ISOLATORMCD2 Module. One isolator circuit is contained in each type ISOLATOR- MCD2


TMT 7 40-2 $29-15 \cdot 127$
Figure 3-44. Type CONTROL-74H87 module, logic symbol and functional diagram.
module (A, fig. 345). The circuit consists of two parts; a light emitting diode (LED) which is optically coupled to a photo diode. Refer to B, figure 345 for a functional diagram of the circuit. Power consists of $+\mathrm{V}_{\mathrm{CC}}$ applied to terminals 1 and 5 . Terminals 3 and 6 have no connections. A high level applied to terminal 2 will develop a low output from terminal 4. When the circuit is activated with a low input to terminal 2, the output at terminal 4 will go to a high level.
k. Type 2A1 Module. Two type N1 gates are located on each type N1 module (fig. 346' These function as inverting OR gates for high inputs. Power is applied by $+\mathrm{V}_{\mathrm{Cc}}$ to terminal 6 and ground to terminal 1.
I. Type DATAROM Module. One 256 bit read only memory, organized as 32 words of eight bits each is contained in the DATAROM module (fig. 347).


Figure 3-45. Type ISOLATOR-MCD2 module, logic symbol and functional diagram.


Figure 3-46. Type N-1 module, logic symbols.
(1) An overriding memory-enable input ( E ) is provided which, when a high level, will inhibit the 32 address gates and cause all eight outputs ( $\mathrm{B}_{0}$ through $B_{7}$ ) to develop a high level.
The addressing of one of the 32 eight-bit words is accomplished through five binary input lines with the memory enable input at a low level.
This enables one of 32 preprogramed eight-bit words to appear on the module output pins.
Truth table for this module as used in this equipment is furnished on figure 821.2.
(2) Power is applied to the module with $+\mathrm{V}_{\mathrm{CC}}$ on terminal 16 and ground on terminal 8.
m. Type ADDRESSROM Module. One 256 bit read only memory, organized as 32 words of eight bits each, is contained in the ADDRESS-ROM module (fig. 347). The ADDRESS-ROM module is identical in construction and operation as the DATA-ROM described above. The only difference between the two modules is the format of the data words that have been preprogramed into the modules. See figure 821.2 for truth table of the ADDRESS-ROM module.


Figure 3-47. Type ROM module, logic symbols.
n. Type DISPLAY1 Module. One solid state numeric display is contained in each DISPLAY1 module (fig. 348). The module stores levels received on a fourwire BCD input and converts these BCD levels to forward bias the appropriate light emitting diodes to visually display the numerals 0 through 9 . Displays will follow changes on the $B C D$ inputs as long as the enable ( E ) line is held low. When the enable line goes to a high level, the display will retain the number at the time of the positive step and will no longer be affected by changes on the BCD input lines. Power is provided with $+\mathrm{V}_{\mathrm{CC}}$ to terminal 7 and ground to terminal 6 .


Figure 3-48. Type DISPLAY-1 module, logic symbol.

## 3-90. Integrated Circuit Latch

a. A special combination of type 7410 OR gates called a latch (fig. 349) is used in the TIG. The latch functions as a flip-flop to register the occurrence of momentary signals. The two OR gates which make up the latch are identified as the set and clear sides of the latch. The 1 output of the latch, which goes high when the latch is set, is produced by the set side and the 0 output,
which goes high when the latch is cleared, is produced by the clear side of the latch.

## NOTE

Compare this circuit with the latch used in the punched tape reader (fig. 317). This latch uses low level pulses for set and clear, thus the 1 and 0 outputs are reversed.
b. To set the latch, both inputs to the clear side must be high, and a low level must occur at either of the two inputs to the set side. The resulting high output of the set side then causes the clear side to produce a low level on the 0 line. This low level reinforces the external input to the set side so that even if the external input goes high, the latch remains set.
c. To clear the latch, both inputs to the set side must be high and a low level must be applied to either clear side input. This action causes the 0 output to go high. Thus, the clear condition is reinforced and remains even after the low level input to the clear side goes high again.


TM 7440-219-15-136
Figure 3-49. Integrated circuit latch, logic symbol.

## 3-91. Operation of Discrete Circuit Logic Elements

a. Discrete Circuit. The operation of the discrete circuit logic element used in the TIG is described below. Logic symbol is given, using typical tagging lines. Schematic diagram and detailed circuit operation of the discrete logic element is given in paragraph 392.
b. Type XMTR1C.The type XMTR1C interface transmitter is located on PC card A1A2 or A4A2 (fig. 350). This circuit converts a low input from the TIG to an open circuit for the CCU. When both inputs go high, a 0 volt level is transmitted to the CCU.


TM 7440-219-15-132
Figure 3-50. Type XMTR-1C interface transmitter, logic symbol.

## 3-92. Detailed Operation of Discrete Circuit Logic Element on PC Card A2

Type XMTR1C interface transmitter (fig. 351), inputs from TIG logic circuits switching between 0 volt and +4.5 volts are coupled through diodes CR1 and CR2 and bias network R1, R2, and R3 to the base of inverter Q1. When either input is 0 volt, Q1 is cut off and supplies an open circuit to the CCU which pulls up the interface line through a load resistor to +6 volts. Since CR1 and CR2 provide an AND function when both inputs have +4.5 volts applied, Q1 will be driven into conduction. This results in a 0 volt output to the CCU.


NOTE:
all resistance values are in ohms.
TM 7440-219-15-133
Figure 3-51. Type XMTR-1C interface transmitter, schematic diagram.

## Section V. ELECTRICAL FUNCTIONING OF TIG

## 3-93. Data Selection Circuits

The data selection circuits gate seven bit characters from either the TIG or the punched tape reader to the CCU. In addition, the data selection circuits gate the odd
parity bit for all data characters.
a. The seven MLPX-74151 modules $\mathrm{Z} 5, \mathrm{Z} 2, \mathrm{Z} 1$, Z4, Z8, Z13, and Z18 on PC card A2 (fig.

8-21.2), select one of eight input sources for bits 1 through 7 respectively. The outputs of these modules (TIG 1A through TIG 64A) are applied to the polar transmitters on PC card A5 (fig. 8-10.2 or 810.3) for transmission over the data interface lines to the CCU. The enable (E) inputs to the MLPX-74151 modules are connected to ground, thus the input levels 20, 21, and 22 determine which input data level will be selected. Refer to the following for determination of input to output line selection:

| Control input lines |  | Output equals input data line |  |
| :---: | :---: | :---: | :---: |
| $2^{2}$ | $2^{1}$ | $2^{0}$ |  |
| 0 | 0 | 0 | $\mathrm{D}_{0}$ |
| 0 | 0 | 1 | $\mathrm{D}_{1}$ |
| 0 | 1 | 0 | $\mathrm{D}_{2}$ |
| 0 | 1 | 1 | $\mathrm{D}_{3}$ |
| 1 | 0 | 0 | $\mathrm{D}_{4}$ |
| 1 | 0 | 1 | $\mathrm{D}_{5}$ |
| 1 | 1 | 0 | $\mathrm{D}_{6}$ |
| 1 | 1 | 1 | $\mathrm{D}_{7}$ |

b. The CONTROL74H87 module Z9 (fig. 821.2) outputs $Y_{1}, \gamma_{2}$, and $Y_{3}$ control the data selection by the MLPX74151 modules. The levels on the B and C inputs to the CONTROL-74H87 module control output $\mathrm{Y}_{1}$ through $Y_{3}$ levels. Outputs $Y_{1}$ through $Y_{3}$ can be all low, equal to the levels applied to inputs $D_{1}$ through $D_{3}$ or all high.
(1) When the TIG front panel ON-LINE/ OFFLINE switch A7S1 (fig. 8-211.1) is in the online position, $+\mathrm{V}_{\mathrm{CC}}$ is applied through S 1 terminals 3 to 2 and a high level is placed on the NOFFLINE signal. Refer to figure 821.2 and note that the NOFFLINE high level is applied by PC card A2 terminal $M$ to the $C$ input on the CONTROL-74H87 module Z9. At several points during the generation of the sixteen character T1 sequence, data characters which are preprogramed into the DATA ROM memory locations are transmitted to the CCU. When this is required, the ADDRESS ROM module Z 10 output $B_{4}$ will develop a low level. When this occurs, note that the output $\mathrm{B}_{4}$ from the Address ROM is applied to the D input of the REG-74195 module Z20. When a signal is applied to the CLK input of Z2O, a flip-flop is cleared and a low level is developed by the $Q_{D}$ output of Z20. This low level is then inverted by OR gate Z14C and applied to the B input of CONTROL74H87 module Z9. Since both the $B$ and $C$ inputs to $Z 9$ module are high, the $Y_{1}$ through $Y_{3}$ outputs will all be low. Thus, the Do inputs to all of the MLPX-74151 modules are enabled. Refer to figure 821.2 and note that the $D_{0}$
inputs of all MLPX-74151 modules are connected to REG74195 modules Z 20 and Z 24 outputs. The $Z 20 \mathrm{Q}_{\mathrm{A}}$ , $\mathrm{Q}_{\mathrm{B}}$, and $\mathrm{Q}_{\mathrm{C}}$ outputs and all outputs from Z 24 will contain the seven data bits for one of the T1 sequence characters when read out of the DATA ROM module Z15. The flip-flops in the Z20 and Z24 REG-74195 modules were loaded with the DATA ROM character at same time the ADDRESS ROM output B, was loaded, as explained above. To summarize, note that DATA ROM character is applied to the TIG output data lines when the CONTROL-74H87 inputs PB and C both have a high level applied.
(2) If the NOFFLINE signal on PC card A2 terminal M and the $\mathrm{Q}_{\mathrm{D}}$ output of REC, Z 20 is high, the CONTROL-74H87 module $Y_{1}$ through $Y_{3}$ outputs will be the same as the 3 least significant bits stored in the register module Z19. The Q1, output of module Z20 is then inverted by OR gate Z14C and a low is applied to the CONTROL74H87 module $\mathrm{Z9}$ input B. ADDRESS ROM outputs $B_{0}$ through $B_{2}$ are stored in the REG74195 module Z19 flip-flops $Q_{D}, Q_{C}$, and $Q_{B}$, respectively. Bits which have been preprogramed into the ADDRESS ROM will cause the outputs of the ADDRESS ROM module Z10 to equal one of the seven binary values from 001 through 111. These levels are passed by the CONTROL-74H87 module $\mathrm{Z9}$ to the select inputs of the seven MLPX-74151 modules. Therefore, one of the six data inputs ( $D_{1}$ through $D_{6}$ ) of the MLPX-74151 modules will be enabled. When the 5th, 6th, and 7th TI characters are to be transmitted, the $D_{1}, D_{2}$, and $D_{3}$ inputs respectively will be enabled. These three positions of the TI sequence are ASCII coded alphabetical characters used to identify the channel designator for a particular terminal location. During installation, jumper wires were connected from either 0 or 1 terminals to the $A, B$, and $C$ terminals which are connected to the $D_{1}, D_{2}$, and $D_{3}$ inputs of each MLPX74151 module. Thus, as the TI sequence is being transmitted, bits preprogramed into the ADDRESS ROM enable transmission of the proper alphabetical character to identify the three channel designator characters. During transmission of the 9th, 10th, and 11th characters of the TI sequence, a numerical count to reflect the message sequence number must be transmitted. Outputs from the MLPX-74153 modules $\mathrm{Z7}$ and Z8 on the PC card A7A1 (fig. 821.3) consist of a binary coded decimal count from one of the three BCD CTR-74160 modules $\mathrm{Z} 1, \mathrm{Z} 2$, or Z 3 . During transmission of the 9th TI sequence character, the count in the hundreds counter Z3 on A7A1 is
gated through MLPX-74153 modules $\mathrm{Z7}$ and $\mathrm{Z8}$ (fig. 821.3) to the $D_{4}, D_{5}$, and $D_{6}$ inputs of the MLPX-74151 modules $\mathrm{Z} 5, \mathrm{Z} 2, \mathrm{Z} 1$, and Z 4 on PC card A2 (fig. 8-2112). At this time, the $D$, input is enabled. In the same manner, the tens counter, PC card A7A1 module Z , is gated on the 10th character by the $D_{5}$, input of the PC card A2 MLPX-74151 modules and the units counter, PC card A7A1 module Z 1 , is gated by the D6 input of the PC card A2 MLPX-74151 modules on the 11th TI sequence character. Since bits 5, 6, and 7 of ASCII coded numerical characters are 110, the $\mathrm{D}_{4}, \mathrm{D}_{5}$, and D6, inputs of the MLPX- 74151 modules $\mathrm{Z}, \mathrm{Z} 13$, and Z 18 (fig. 8-21-2) are wired to 1 and 0 as required.
(3) The selection of the D inputs to the PC card A2 MLPX-74151 modules can be accomplished in one of two ways. First-after the last TI sequence character has been generated, the ADDRESS ROM module Z10 outputs $B_{0}, B_{1}$, and $B_{2}$ will all remain high. These levels are applied through the REG-74195 module Z19 and the CONTROL-74H87 module Z9 to apply all highs on the $2^{0}, 2^{1}, 2^{2}$ inputs to the MLPX-74151 modules on PC card A2. Therefore, the $D_{7}$ inputs are enabled. When data characters are read from the punched paper tape, the data is stored in the data register on PC card A7 (fig. 812.1) (para 3-63), The outputs from data gates on PC card A7 are then applied to the D, inputs of PC card A2 MLPX-74151 modules. The second manner in which the punched tape reader data can be gated through the PC card A2 MLPX -74151 gates is in the case of TIG off-line operation. When the ON-LINE/OFF-LINE switch A7S1 (fig. 8-1.1) is in the off-line position, a low level is developed on the NOFFLINE signal by the switch terminal 1 to 2 contacts. This low is then applied to input C of the CONTROL-74H87 module Z9 on PC card A2 [fig. 8-21.2) and to OR gate Z14C which inverts the level and a high is placed on the B input to the $\mathrm{Z9}$ module. This high on the B input and the low on the C input will cause the CONTROL-74H87 module $\mathrm{Z9}$ to generate all high outputs regardless of the levels on the $D_{1}$ through $D_{3}$ inputs. The high $Y_{1}$ through $Y_{3}$ outputs will then enable the MLPX-74151 modules to gate punched tape reader data through the $D_{7}$ inputs to the interface drivers on PC card A5.
c. The PAR GEN-74180 module Z23 on PC card A2(fig. 8.21.2) samples the seven data line outputs of
the MLPX-74151 modules. Since the EVEN input to module Z23 is connected to a high and the ODD input is connected to ground, the SUM ODD output will generate an odd parity bit on the TIG 128A signal line. Thus, if the TIG 1A through TIG 64A lines have an even number of high level bits, the TIG 128A signal will be high. Also, if TIG 1A through TIG 64A have an odd number of high levels, the TIG 128A signal will be low. The TIG 128A signal is applied to PC card A5 (fig. 8-10.2 or 8-10.3) polar transmitter for transmission to the CCU. Note on figure 8-21.2 that the output of the PAR GEN-74180 module at PC card A2 terminal AA is connected to the output of AND gate Z3A at PC card A2 terminal 11. This connection functions as a WIRE-OR as illustrated on figure 8-2112. Thus, if either terminal AA or terminal 11 have a low level, the low will be transmitted to the CCU by the interface transmitter on PC card A5. This WIREOR along with inverter Z3B, AND gate Z3A, and PAR GEN-74180 module Z23 function to detect the majority of parity errors read from the ASCII coded paper tape. The level of the parity bit (signal 128A) from PC card A7 ffig. $8-12.1$ ) is applied through inverter Z3B on PC card A2 (fig. 8-21.2) to AND gate Z3A. The other input to AND gate Z3A is the signal TIG SELA on PC card A2. The signal TIG SELA is a high level only during the time the punched tape reader data is being transmitted to the CCU. Thus, during TI sequence generation the output of AND gate Z3A is always high and the WIRE-OR function of terminals AA and 11 will follow the output of the PAR GEN-74180 module Z23. When the TI sequence is completed, the TIG SELA signal will go to a high level enabling AND gate Z3A thus allowing both inputs to the WIRE-OR function of terminals AA and 11 to develop the parity bit. Under normal operation both inputs to the WIRE-OR should have the same level and correct parity is transmitted to the CCU. However, if the parity bit to the CCU should be transmitted as a high level, and a low level is provided by the punched tape reader data register parity bit, the low level will be transmitted to the CCU, causing the CCU to detect a parity error thus stopping the operation and canceling the message transmission. It is possible for a character to be incorrectly sent to the CCU without detection of parity error. This would, occur when the seven ASCII data bits of the character have an even number of "1's" but one of the data bits is misread. Thus, the PAR GEN-74180 module Z23 will develop a low output

## Change 4 3-80

and an incorrect character with valid parity is sent to the CCU.

## 3-94. TIG Control Circuits

The TIG control circuits are contained on PC card A2 (fig. 8-211,2). These circuits contain several functional units to generate timing and reset signals and to provide mode and sequence control of the TIG operation. Detailed theory of operation of the control circuits is provided in 円aragraphs 3-95 through 3-98. Refer to figure $3-52$ for timing diagram of the control signal generation.

## 3-95. TIG Timing Generator

The TIG timing generator controls the timing sequence for transmission of each character during the TI sequence. Each cycle lasts for 6 counts of a $104-\mu \mathrm{sec}$ clock period or a total of $624 \mu \mathrm{sec}$. The timing generator consists of six flip-flops connected as a shift register and associated start control gates.
a. To start the timing generator, an active high level signal must be received from the CCU on both the select and the step/data acknowledge interface lines. When this occurs, high levels are applied from PC card A4 ffig. $8-9.2$ or 8-9.3) to AND gate Z17A inputs on PC card A2. The SDA line is applied directly and the SELA line is gated through inverters Z26A and Z26D. If the generator is not in a cycle, the third input to AND gate Z17A will be a high level. The low output of AND gate Z17A is then applied to the D input of flip-flop Z12B which is in a set state when the timing generator is not cycling. Thus, on the next positive step on the 9.6 KC clock line from PC card A1, the Z12B flip-flop will clear. The now high Q output of Z 12 B is applied to the J and. K inputs of the four stage REG74195 module Z22. The positive step of the next four 9.6KC clock pulses will sequentially set the four flip-flops in the Z22 module. Each of the four REG74195 module flip-flops will remain set for one clock pulse since the QA output clears flip-flop Z12B through OR gate Z11D. (See timing diagram in figure 3-52). After the positive step of the fifth clock pulse, the Z22 module $Q_{D}$ output will be low. The Z 22 module $\mathrm{Q}_{\mathrm{D}}$ signal is applied to the flip-flop Z12A CLK input which was set on the second clock pulse by the high level Z 22 module QA output through invertor Z11C. When the sixth 9.6KC clock pulse occurs, the $Z 22$ module $Q_{D}$ output will go high. Since flip-flop Z12A input D is connected to ground, the resulting positive step on the CLK input will clear flip-flop Z12A. Note that the flip-flop Z12A output Q
is applied to the start control AND gate Z17A. Thus, the maximum cycle rate of the timing generator is one character every $624 \mu \mathrm{sec}$.
b. Outputs from the timing generator are applied to the TIG data strobe gate Z27B, EM control gate Z14B and sequence control registers $\mathrm{Z} 19, \mathrm{Z} 20$, and Z 24 .

## 3-96. Reset Gates

The reset gates are used to reset the TIG upon power on and at the end of each message. The reset gates consist of AND gate Z17B and OR gates Z11D and Z17C.
a. In the on-line mode, $+\mathrm{V}_{\mathrm{cc}}$ is coupled through terminals 1 to 2 of the ON-LINE/OFFLINE switch A7S1 (fig. 8-1.1) to develop a high level on the NOFFLINE signal. The NOFFLINE high level is applied to PC card A2 partially enabling AND gate Z17B. The other input to AND gate Z17B is from OR gate Z17C which will have a high output if a low is placed on the NAST line from PC card A4 or on the NRCS line from PC card A14. The alarm stop signal NAST is generated on PC card A15 (fig. 8-20,1) and will develop a low level under message cancel, tape out alarm, tape motion alarm, and invalid alarm conditions (para 3-66). The not remote continuous step signal NRCS is also generated on PC card A15 and will normally develop a low level under initial power-up of the punched tape reader and also upon detection of the end of a message (para 3-39) Once a low level is placed on the NRCS line, it will remain low until the detection of the first valid character of the next message read from the paper tape.
b. The low NAST or NRCS signals are double inverted by OR gates Z17C and Z11D on PC card A2 to set the timing generator Z12B flip-flop. The low output from AND gate Z17B is applied to the TIG/PTR mode latch Z21C to place it in the TIG data mode when in TIG on-line mode. The low output from AND gate Z17B is also applied to clear the timing generator modules Z22 and Z12A and the sequence control registers $\mathrm{Z} 19, \mathrm{Z} 20$, and Z24.

## 3-97. Mode Control

In the TIG on-line mode, the TIG/PTR mode control latch and OR gates Z21A and Z21C, are used to control transmission of data to the CCU consisting of the TI sequence characters or data read by the punched tape


TM7440-219-15-138
Figure 3-52. TIG control circuits, overall timing diagram.
reader. Outputs from the latch are applied to the TIG select and data strobe circuits to control punched tape reader operation and data strobe generation to the CCU. Refer to timing diagram (fig. 3-52) illustrating signals in following description:
a. Before the start of each message, the TIG/PTR mode latch is cleared to TIG mode by a low input to OR gate Z21C from the reset gates. In this state, the high output of OR gate Z21C inhibits generation of a high TIG SELA signal to the PC card A15. This signal prevents punched tape reader operation until the completion of the transmission of the Tl sequence. A high level from latch Z21C is also applied to AND gate Z27B. This enables the high output from the timing generator Z22 module output $Q_{C}$ to be gated through AND gate Z27B and OR gate Z27C to place a high level on the TIG DST line to the CCU through PC card AS. The low output from OR gate Z21A is applied to AND gate Z27A thus inhibiting any high DST data strobe signals received from PC card A14.
b. Once the TI sequence has been completed, each cycle of timing generator will cause a preprogramed character to be read out of the DATA ROM module Z 15 which contains a 1 bit in the B5 position (para 3-98). This high level in the DATA ROM B5 position will then be stored in the sequence control register module Z24 flip-flop Q., . When this occurs, the Z24 module in output will go low causing the TIG/PTR mode latch Z21A and Z21B to change state to reflect the PTR data mode. Now the TIG SELA gate is enabled and the SELA signal from PC card A4 is gated through inverter Z26B, AND gate Z26A and applied to the PC card A15 to allow punched tape reader operation. The high DST pulses generated on PC card A14 can now be gated through AND gate Z27A, and OR gate Z27C to place high pulses on the TIG DST line to the CCU through the polar transmitter on PC card A5. At the same time, the low output of the TIG/ PTR mode latch OR gate Z21C to AND gate Z27B to inhibit generation of TIG DST pulses from the timing generator Z 22 module outputs.
c. In the TIG off-line mode, the low NOFFLINE signal to OR gate Z21B forces the TIG/ PTR latch into the PTR mode.

## 3-98. Sequence Control

The sequence control circuits on PC card A2 provide for the selection of Tl character sequence transmission, ASCII coded alphabetical and machine function characters, and ACP 127 start position strapping option. These circuits consist of three REG-74195 modules, two

ROM modules, and start patch circuitry. The three REG-74195 modules Z19, Z20, and Z21 function as a twelve bit storage register. The DATA ROM Z15 contains the preprogramed ASCII coded characters and PTR mode control Bit. The ADDRESS ROM Z10 contains preprogramed binary addresses to control character sequence. The start position circuitry consists of a dual MLPX-74153 module Z6 and associated gates and strapping terminals.

Should future requirements necessitate a change in the sequence of transmission, the modification can be made by simply removing present ROM modules and replacing them with new modules having different programs. The twelve pull-up resistors R5 through R16 are used to provide a high level output when a logical I is stored in the read only memory.

## CAUTION

Since modules Z10 and Z15 on PC card A2 have different programs, they are not interchangeable.
a. DATA ROM Module Z15. The DATA ROM module is an addressable 256 bit read only memory arranged in 32 words of eight bits each, however only 18 words of seven bits each are used. The enable (E) input is connected to ground, allowing outputs B0 through B6 to reflect the data character stored in the address location selected by the binary $A_{0}$ through $A_{4}$ inputs. Refer to the ROM program chart on figure 8-21. 2 for the contents of the characters programmed into the various memory addresses. Observe that the ROM program table is arranged in the order of the Tl sequence transmission. Refer to the memory location column which shows both the decimal location and the binary values applied to the $A_{0}$ through $A_{4}$ inputs to the DATA ROM module. Also note the DATA ROM output $B_{5}$ has a dual function; in all sixteen Tl character locations, $\mathrm{B}_{5}$ is a 0 indicating "TI data function" but in the two locations used during transmission of the PTR data characters a " 1 " bit is placed in the $B_{5}$ position. This high level $B_{5}$ output is applied to the sequence register module Z 24 flip-flop $D$. The low level inverted $Q_{D}$, signal is then applied to the TIG/PTR mode latch OR gate Z21A to place the TIG into PTR data mode.
b. ADDRESS ROM Module Z10. The ADDRESS ROM module is an addressable 256 bit read only
memory arranged in 32 words of eight hits each, however only 18 words of five bits each are used. The enable ( E ) input is connected to ground allowing outputs $B_{0}$, through $B_{4}$ to reflect the address word stored in the address location selected by the binary $\mathrm{A}_{0}$ through $\mathrm{A}_{4}$ inputs. Refer to the ROM program chart on figure 8-2112 for the contents of the bits programmed into the various memory addresses. Observe that the ROM program table is arranged in the order of the TI sequence transmission. If you refer to the memory location column, you can identify both the decimal location and the binary values applied to the A, through A, inputs of the ADDRESS ROM module. The contents of the ADDRESS ROM memory locations perform two prime functions as follows:
(1) Provides the 5 bit binary memory address of the next memory word to be used. For example: refer to the ROM program table in figure 8-212 and note that the contents of first ADDRESS ROM word (ADDRESS 00000 ) is 00001 which is the location where the second memory N word is stored in the DATA and ADDRESS ROM's.
(2) ADDRESS ROM output $B$ controls the mode of operation of the CONTROL-74H87 module $\mathrm{Z9}$. The output B, is stored in sequence register module Z20 $Q_{D}$ flip-flop which, in turn, provides an inverted input to the CONTROL-74H87 module Z9 input B through OR gate Z14C. When the ADDRESS ROM output B, is low, the DATA ROM outputs are applied to the CCU intetrface lines through the seven MLPX-74151 modules para 3-936(1)). When the ADDRESS ROM output B, is high, data gated to the interface line by the seven ML, PX-74151 modules will be the channel designator for a particular terminal, the channel sequence number from the counter on the TIG front panel, or data characters read by the punched tape reader (para 3-93c(2) and (3)).
c. Sequence Control Register. The sequence control register functions as a 12 bit flip-flop storage register to store the data read out of the ADDRESS and DATA ROM's. The sequence control register consists of the three REG-74195 modules Z19, Z20, and Z24 on PC card A2. Upon power up and at the end of each message the low level to the CLR input the three modules from the AND gate Z17B will reset all 12 flipflops to the clear state. The flip-flops will assume the state indicated by the ROM outputs on the positive step of the CLK input from the timing generator.

The $\mathrm{S} / \mathrm{L}$ input is connected to ground to enable parallel loading of the register by the CLK input. Refer tofigure

3-52 overall timing diagram which illustrates an example of the timing relationship of ROM outputs to loading of the sequence control register. Outputs from the sequence control register perform the following functions:
(1) Module $Z 24$ output $Q_{D}$ is applied to the TIG PTR mode latch Z21A to start the PTR data mode after the last TI sequence character has been transmitted.
(2) Module $Z 24$ outputs $Q_{A} Q_{B} Q_{C}$, and $Q_{D}$ and module Z 20 outputs $\mathrm{Q}_{\mathrm{A}}, \mathrm{Q}_{\mathrm{B}}$, and $\mathrm{Q}_{\mathrm{C}}$ are applied to the data selection circuits to enable transmission of TI sequence characters stored in the DATA ROM.
(3) Module Z20 output $\mathrm{Q}_{\mathrm{D}}$, and module $\mathrm{Z19}$ outputs $Q_{A}$, and $Q_{C}$ are applied to AND gate Z21B to provide end of medium detection.
(4) Module $Z 20$ output $Q_{D}$, is applied to data selection circuit OR gate Z14C to provide selection of data from either the DATA ROM or from other sources.
(5) Module $Z 19$ outputs $\mathrm{Q}_{\mathrm{B}}, \mathrm{Q}_{\mathrm{C}}$, and $\mathrm{Q}_{\mathrm{D}}$ are applied to data selection circuit CONTROL 74 H 87 module Z9 to control selection of transmission of characters other than DATA ROM storage.
(6) Module $Z 19$ output $Q_{C}$ and $Q_{D}$, are applied through inverters Z16A and Z16B to the counter selection circuits on PC card A7A1 (fig. 8-21.3) to determine which digit of the message sequence count is to be gated to the interface line during transmission.
(7) Module Z 20 output $\mathrm{Q}_{\mathrm{D}}$ and module $\mathrm{Z19}$ outputs $Q_{A}, Q_{B}, Q_{C}$, and $Q_{D}$ are applied to the address inputs and start patch of the DATA and ADDRESS ROM's to enable selection of the next character to be transmitted.
d. Start Strap. The first three characters of the TI sequence identify the ACP-127 start of message. The start strap enables optional transmission or nontransmission of part or all of the three characters. Thus, the TI format may begin with character $1,2,3$, or 4. The start circuits consist of AND gates Z3C, Z11A, Z11B, and MLPX-74153 module Z6, plus associated standoff terminals. The AND gates Z3C, Z11A, and Z11B function as a "start TI sequence" decoder. Either upon power-up or after the end of each message, the sequence control register is cleared.

This enables all decoder inputs causing the output from Z3C to go low. Once the TI sequence has started, at least one input to AND gates Z11A or Z11B will be high, thus, AND gate Z3C will develop a high level. On the first character of the TI sequence only, the low levels on $2^{0}$ and $2^{1}$ inputs to module $Z 6$ will cause the strapped inputs $1 \mathrm{D}_{0}$ and $2 \mathrm{D}_{0}$ to be gated to the 1 Y and 2 Y outputs. On all other character transmissions, the high level on the $2^{0}$ input and low level on the $2^{1}$ input gates the ADD $2^{0}$ and ADD $2^{1}$ lines through the $1 D_{1}$ and $2 D_{1}$ inputs to the 1 Y and 2 Y outputs. Upon installation of the TIG, it is necessary to put jumper wires from the terminals $2^{0}$ and $2^{1}$ to either terminals 0 or 1 on PC card A2. The following identifies patches to select desired start positions:

| Desired TI sequence <br> start position | Strap terminal <br> $2^{0}$ TO- | Strap terminal <br> $2^{1}$ TO- |
| :--- | :---: | :---: |
| First character-Z | 0 | 0 |
| Second character -C | 1 | 0 |
| Third character-Z | 0 | 1 |
| Fourth character -C | 1 | 1 |

The 1Y and 2Y outputs of MLPX-74153 address are applied to ROM modules Z10 and Z15 as the two least significant bits of memory address. Once the first character for memory (any of the four characters identified in above table) has been loaded into the sequence control register, the ADDRESS ROM module will then sequentially transmit the remaining characters in the TI sequence.

## 3-99. End of Medium

The last character of the TI sequence to be transmitted is a NUL character which is accompanied by an active level on the EM interface control line. In addition, during transmission of the EM function, the message sequence counter on the TIG control panel must be incremented by one. The circuits performing these functions are on PC card A2 (fig. 8-212) consisting of AND gates Z21B and Z14B, inverter Z16, and neutral discrete circuit interface transmitter XMTR-1C.
a. When the NUL character in ROM location 9 is loaded into the sequence control register, AND gate Z21B is enabled. The inverted output of AND gate Z21B through inverter Z16C is a high level partially enabling AND gate Z14B and XMTR-1C. When the TIG is in the on-line mode, the high level NOFFLINE signal is also applied to both AND gate Z14B and the XMTR1C
interface transmitter. A high level on both inputs to the XMTR-1C will cause a 0 -volt level on the end of medium (EM) interface line to the CCU. Refer to timing diagram figure 3-52. The EM line will remain low until the TIG timing generator cycles in response to the CCU requesting the next character. At this time, the output from AND gate Z21B will be a high level and the EM interface line will revert to an open.
b. AND gate Z14B also is further enabled by timing generator module Z22 flip-flop $Q_{c}$ output. Thus, 208 $\mu \mathrm{sec}$ after the EM line develops an active level, a 104 $\mu s e c$ low pulse will be developed on the NEM PULSE line. This pulse is applied to the counter clocking circuitry on the TIG control panel PC card A7 (fig. 821.3) which increments the message sequence counter in both the A7 and A8 TIG assemblies.

## 3-100. On-Line/Off-Line Control

The ON-LINE/OFF-LINE switch A7S1 provides operator control over the transmission or nontransmission of the TI sequence at the start of each message. Depending upon the position of the switch A7S1 (fig. 8-1,1), either $+V_{C C}$ or ground is coupled through the switch to develop a high or a low level on the NOFFLINE signal line. This line is applied to PC card A2 to enable TI sequence generation when the line has a high level. TI sequence generation is inhibited when the NOFFLINE signal is at a low level. The A7S1B contacts provide for a 15 VAC RTN path to the TIG ON indicator A7DS1. The TIG ON indicator is illuminated when the ON-LINE/OFFLINE switch is in the ON-LINE position.

## 3-101. Message Sequence Counter

The message sequence counter maintains a record of the number of messages transmitted from the terminal. The counter is incremented by one during the transmission of the TI sequence. The count stored in the message sequence counter is also transmitted as a part of the TI sequence. The counter resets to 000 upon power-up, however, TIG front panel controls enable operator to manually load any number from 000 to 999 into the counter. In those terminals having dual TIG assemblies installed, the message sequence counter in both TIG assemblies will be incremented regardless of which punched tape reader/ TIG unit is transmitting the message. In this case however, both counters must initially be loaded to the same count to insure transmission of the proper message sequence numbers when reading from both punched tape readers. The
message sequence counter circuits are all contained on the TIG assembly front panel (fig. 81.1) or on the PC card A7A1 fig. 8-21.3) which is mounted to the TIG assembly front panel. All integrated circuit components on this PC card plug into dual ill-line sockets for ease of maintenance.
a. Binary Coded Decimal Counter. The three stare binary coded decimal counter on PC card A7A1 consists of three BCD CTR-74160 modules Z1, Z2, and Z3. Module Z 1 functions as the units counter, module Z 2 is the tens counter, and module $\mathrm{Z3}$ is the hundreds counter. Upon power-up a positive pulse from PC card AI is coupled through inverter Z6A to reset all outputs of the counter to a low level. Capacitor C2 functions as a noise filter to prevent accidental clearing of the counter. If the two enable ( E ) inputs to the counter module are high, the counter modules will increment on a positive step of the CLK input. Note the E inputs of module Z1 are connected to $+\mathrm{V}_{\mathrm{CC}}$ enabling this module to step on each clock pulse. The CR' output of module Z1 is high only during the count of 9 . Since this CRY output is connected to the E inputs of module Z 2, the tens stage can be stepped only on every 10th clock pulse. In a similar manner, module Z3 can be stepped only on every 100th clock pulse. The three stages of the counter can also be manually preset by the counter load control circuits as described below. The binary coded outputs from the counter modules are applied to the counter selection gates and to the visual display DS2.
b. Visual Display DS2. The three visual display modules DS2U, DS2T, and DS2H are all mounted in a single dual in-line socket on PC card A7A1.Note that figure 8-21.1 identifies both socket and individual module terminal numbers. In addition, the display DS2 is mounted on the reverse side of the PC card to enable observation through the aperature in the TIG assembly control panel.
c. Counter Clocking. During the transmission of the last TI sequence character to the CCU, the low level $104 \mu \mathrm{sec}$ NEMPULSE is generated on PC card A2 and is applied through OR gate Z5A to the CLK input of the three counter modules $Z 1, Z 2$, and $Z, 3$ on PC card A7A1. The positive pulse on the CLK inputs to these modules will increment the three stage counter by one. Refer to If below for description of incrementing counter from other TIG.
d. Counter Load Control. The counter load control enables manual presetting of the message sequence counter. The circuit consists of latch ZS5B and Z5C, Inverter Z6B, OR gates Z9A and Z5A on PC card A2 (fig. 8-21.1) the TIG front panel pushbutton

LOAD switch A7S3 (fig. 8-1.1) and the three section MANUAI, UPDATE thumbwheel switch A7S2. (fig. 81.1). Each of the thumbwheel switches have 10 positions and are connected to one stage of the binary coded sequence counter. Each section of the switch receives power from PC card A7A1 and provides a four line binary coded decimal output. The binary code levels on the output lines depend upon which one of the ten positions to which the switch is manually set. The output of each switch is applied to the $2^{\circ}, 2^{1}$, and $2^{3}$, inputs of the respective counter module. Normally a high output from latch Z5B output is applied to the LOAD inputs of modules $\mathrm{Z} 1, \mathrm{Z2}$, and Z 3 to inhibit the switch outputs from affecting counter module operation. To manually preset the counter, depress the LOAD pushbutton switch A7S3. Ground is then coupled through the A7S3 common to normally-open contacts to change the state of latch Z5B and Z5C. Resistors R1 and R2 are connected to $+\mathrm{V}_{\mathrm{Cc}}$ to insure a high level is generated from the open side of the switch. The low level from Z5B will set the counter modules when a positive transition occurs on the CLK inputs to modules $\mathrm{Z} 1, \mathrm{Z} 2$, and Z 3 . This is accomplished by a low level output from latch Z5B gated through inverter Z6B, OR gate Z9A, and OR gate Z5A to apply a positive pulse to the counter module CLK inputs. This positive pulse causes the four flip-flops in each BCD CTR74160 to assume the state indicated by the thumbwheel switches. Note that there is a time delay between the time the low level LOAD input is detected by the counter modules and the time the positive CLK input is applied. This is caused by the tiransistion time of the positive pulse from latch Z5B through the inverter Z6B, OR gates Z9A and Z5A, and the effect of the capacitor C3. If the TIG 'punched tape reader is selected by the CCU, manual loading of the counter is inhibited. A low level NSELECT signal from PC card A2 is applied to latch OR gate Z5B on PC card A7A1. When this signal is present, a low level output from latch Z5B is inhibited even if the pushbutton LOAD switch A 7 S 3 is depressed.
e. Counter Selection. The 9th, 10th, and 11th TI sequence characters to be transmitted consist of numerical ASCII characters indicating the

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contents of the hundred counter Z 3 , tens counter Z2, and units counter Z1. Outputs from each of the four flip-flops in the three counter modules on PC card A7A1 are applied to the two MLPX74153 modules $\mathrm{Z7}$ and Z 8 . Address bits from the ADDRESS ROM module Z10 on PC card A2 (fig. 8-21.2) are applied through sequence control REG-74195 module Z19, inverters Z16A, Z16B to PC card Z7A1 counter selection modules Z7, Z8 inputs $2^{0}$ and $2^{1}$. Therefore, when inputs $2^{1}$ and $2^{\circ}$ are both high during the 9th TI sequence position, the counter selection module outputs reflect the count in the hundreds counter module Z3. In a similar manner, the state of the tens counter is gated for the 10th character and the units counter is gated for the 11th character.
f. Increment Other TIG. In dual TIG installations, a low NEMPULSE signal must also increment the message sequence counter in the other TIG. This circuitry consists of inverters Z6C and Z6D and ISOLATOR-MCD2 module Z4 on PC card A7A1 (fig. 821.2). The active low level NEMPULSE from PC card A2
is double inverted by inverters Z6C and Z6D and applied to terminal board A7TB1 terminal 5 (filg. 8-1.1). Also $+\mathrm{V}_{\mathrm{CC}}$ is connected to terminal board A7TB1 terminal 4 to provide power for the ISOLATOR-MCD2 module $Z 4$ in the other TIG. The NINTIG signal on terminal board A7TB1 terminal 5 is connected to terminal board A8TB1 terminal 8 (fig. 8-1 1). The $+\mathrm{V}_{\mathrm{CC}}$, signal on terminal board A7TB1 terminal 4 is connected to terminal board A8TB1 terminal 7. In a similar manner A8TB1-5 is connected to A7TB1-8 and A8TB1-4 is connected to A7TB1-7. Thus, the LED VCC signal from the other TIG is received on terminal board TP, 1 terminal 7 and is applied to the ISOLATORMCD2 module Z4 (fig. 8-21.2) through current limiting resistor R3. When a low level pulse is received from the other TIG on terminal board TB1 terminal 8, a high level pulse is developed on the ISOLATOR-MCD2 module Z4 output terminal 4. This pulse is then gated through OR gates Z9A and Z5A to the BCD CTR-74160 CLK inputs to increment the message sequence counter by one.

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## CHAPTER 4 <br> MAINTENANCE INSTRUCTIONS

## Section I. GENERAL

## 4-1. Scope of Maintenance

a. This chapter includes instructions for performing preventive and corrective maintenance procedures on all major assemblies. subassemblies, and components (except PC cards) of the punched tape reader. Maintenance procedures for the PC cards are provided in chapter 5.
b. Maintenance of the punched tape reader includes the following:
(1) Preventive maintenance (paras 4-3 through 4-8.
(2) Troubleshooting paras 4-9 through 4-15).
(3) Removal and replacement (paras 4-16 through 4-43.
(4) Repairs and adjustments (paras 4-44 through 4-62).

## 4-2. Tools, Materials, and Test Equipment Required

a. Tools and Test Equipment. Refer to appendix C for a list of the tools and test equipment required for maintenance of the punched tape reader.
b. Materials. The following maintenance mate
rials are required in addition to the maintenance materials furnished as part of the tool kits listed in appendix C
(1) Lint-free cleaning cloth, NSN 8305-00-267-3015.
(2) Fine sandpaper (0000), NSN 5350-00-235-0124.
(3) Primer, zinc chromate, FED SPEC TT-P-664, NSN 8010-00-

936-3372 (pt.)
(4) lacquer, semigloss, blue (No. 25184 per FED STD 595), NSN 8010-00-721-9753 (pt).
(5) Enamel, semigloss, gray (No. 26492 per FED STD 595), NSN 8010-00-087-0109 (qt).
(6) Enamel, semigloss, black (No. 27038 per FED STD 595), NSN 8010-00-844-4792 (qt).
(7) Trichloroethane, FED SPEC O-T-620, Type I, NSN 6810-00-292-9625 (qt), or NSN 6810-00-664-0387 (gal)
(8) Trichlorotriflorethane (Freon TF), MIL-C-81302B, Type II, NSN 6850-00-033-8851 (1 gal).
(9) Sealing compound, retaining (LOCTITE, Grade A), NSN 8030 00-081-2339 (1 gal)
(10) Scaling compound, retaining (LOCTITE, Grade E), NSN 8030-00-081-2328 (10CC btl).
(11) Primer, sealing compound (LOCTITE, Grade T), NSN 8030-00-145-0001 (6 oz can).
(12) Compound, antiseize, MIL SYMB A-907C, NSN 8030-00-2921102 (8 oz).
(13) Adhesive (GLYPTAL No. 1153), NSN 5970-00-162-7523 (pt)
(14) Coater, filter, NSN 4130-00-860-0042 (pt)
(15) Compound, silicone (heat sink), Dow corning 340, NSN 6850-00-181-6995 (2 oz), or NSN 6850-00-927-9461 (5 oz).
(16) Oil, lubricating, Grade 0E-30, MIL SYMB 0-180, NSN 9150-00-265-9433 (qt)
(17) Oil, lubricating, general purpose, nondetergent, MIL SYMB 2110TH, NSN 9150-00-985-7235 (pt).
(18) Groase, silicone, Dow Corning No. 44, NSN 9150-00-257-5358 (8 oz).

## Section II. PREVENTIVE MAINTENANCE

## 4-3. Scope of Preventive Maintenance

a. Preventive maintenance is the systematic care, inspection, and servicing of the punched tape reader, to maintain it in serviceable condition, prevent breakdowns, and assure maximum operational capability. Preventive maintenance includes inspection, testing, and replacement of parts, subassemblies, or units that inspection and tests indicate would probably fail before the next scheduled periodic service.
b. The preventive maintenance checks and services procedures outline functions necessary to maintain the punched tape reader in good operating condition.
c. Weekly and monthly preventive maintenance periods are specified as follows: A week and a month are defined as approximately 7 and 30 calendar days of 8houraday operation, respectively. If the punched tape reader is operated 16 hours a day, the weekly and monthly preventive maintenance checks and services
should be performed at 4day and 15day intervals, respectively. Adjustment of the preventive maintenance interval should be made to compensate for any unusual operating conditions.
d. Refer to paragraph 13d for information on the records and reports of preventive maintenance.

## 4-4. Daily Preventive Maintenance Checks and Services

Press LAMP TEST switch and check to be sure that pressing the switch causes all indicators on the control panel to light (except POWER indicators). Clean paper lint and dust from the top of the tape deck assembly as follows:
a. Press the button on the front of the read head to permit the tape holddown assembly to tilt upward.
b. Use a soft brush or a hand vacuum cleaner
to remove lint and dust from the tape track.

## 4-5. Weekly and Monthly Preventive Maintenance

a. Weekly. Replace the cabinet air filter with a clean air filter. When time permits, clean the removed filter and install it during the next weekly maintenance procedure (para 48.1).
b. Monthly. Remove the bottom cover (10, fig. 412) to gain access to the read head starwheels and the starwheel levers (fig. 36). Clean paper lint and dust from the starwheels and starwheel levers with a soft brush or a hand vacuum cleaner.

## NOTE

Removal of paper lint and dust from starwheels and starwheel levers must be accomplished on a regular monthly basis, or after 250 hours of operation, to prevent contamination of electrical contacts. Do not blow or use air pressure to remove dust from the starwheel area. If a soft brush is used to dislodge dirt, always brush away from the contact area and use the vacuum cleaner after brushing.

## 4-6. 250-Hour, 1000 -Hour and 2000 -Hour Preventive Maintenance Checks and Services

a. 1000-Hour Checks and Services. Remove 2 screws (6, fig. 412) and lift the assembled fan and capstan drive guards to gain access to the capstan drive mechanism (64). Use the hand vacuum cleaner to remove loose dirt from the capstan drive mechanism and the motor and fan. Inspect Blower B-1 blades for dirt buildup. If blades are caked with dirt, disassemble blower assembly and clean.
b. 250Hour Checks and Services. Clean and lubricate the capstan drive mechanism (para 48).
c. 2000 Hour Checks and Services. Remove the capstan drive mechanism and inspect thoroughly for worn parts. Replace worn parts as required.
Clean, lubricate, and adjust the mechanism as described in this chapter and replace in the assembly.

| $\begin{aligned} & \text { Item No. } \\ & \text { fig. } 4-1 \end{aligned}$ | Lubrication point | Lubrication interval | Method and quantity |
| :---: | :---: | :---: | :---: |
| 1 | Bearings on shafts and idler gears of capstan drive mechanism. | Every250 hours of operation. | Apply 1 or 2 drops of Bardol BOA 30. |
| 2 | Escapement armature felt pad. | Every 1,000 hours of operation. | After wiping escapement armature and adjacent pole face with lint-free cloth, apply I or 2 drops of <br> SAE 30 <br> oil to the felt pad. <br> Caution. Do not spill oil on adjacent friction clutch. |
| 3 | Friction clutch escapement teeth | Every 1, 000 hours of operation. | Clean previous lubricant off the friction clutch escapement teeth. Relubricate escapement teeth with a light coat of silicone grease, Dow Corning No. 44. |
| 4 | Motor | Every 4, 000 hours of <br> operation or 2 years, whichever occurs first. | Apply 8 drops of lubricating oil, general purpose <br> (2110TH) into the oil-hole on each side of the motor. |

### 48.1 Cleaning Cabinet Air Filter

Remove loose dust and dirt from the cabinet air filter after each 50 hours of operation ( a and b below). Wash and recoat the filter after each 250 hours of operation (c below).
a. Pry the upper corners of the grill assembly forward slightly and lift the assembly upward to remove it from the cabinet. Lift the exposed filter upward slightly and then forward to remove it from the equipment cabinet.
b. Use a hand vacuum cleaner to remove loose dust and dirt from both sides of the filter.
c. Wash and recoat air filter as follows:
(1) Vacuum the air filter using the procedure outlined in step b above.
(2) Prepare a solution of warm water and detergent in a suitable container large enough to permit immersion of the filter.
(3) Place the filter in the solution of warm water and detergent; allow the filter to soak for several minutes in the solution.
(4) Thoroughly wash the filter by agitating, raising and lowering the filter in the solution, thus permitting the solution to run through the woven filter material.
(5) Thoroughly rinse the filter in clean, clear water using the same procedure as was used for washing.
(6) Shake the filter to remove as much water as possible; then set filter aside to drain and dry at room temperature or use a low pressure source ( 15 psi ) of dry compressed air to dry the filter.
(7) Hold a spray can of Coater, Filter (FSN 41308600042 ) about 12 inches from the dry filter and press the button while moving the can to apply an even thin coat to the filter. Then apply an even thin coat to the opposite side of the filter.
Repeat this procedure to apply a total of three thin coats to each side of the filter.
d. To install the clean air filter, reverse the removal procedure (a above).


Figure 4-1. Capstan drive mechanism and motor lubrication points.

## Section III. TROUBLESHOOTING

## 4-9. Use of Troubleshooting Charts

a. Detailed procedures for troubleshooting a faulty punched tape reader are presented in two troubleshooting charts (Daras 4-10 and 4-11). Refer to the troubleshooting chart in paragraph 410 to localize the fault to one of the components of the punched tape reader and to isolate the fault to the defective part or maladjustment of all components except the power supply. Refer to the troubleshooting chart in paragraph 4-11 to locate troubles in the power supply.
b. When starting a troubleshooting procedure, place the punched tape reader into operation and note the first apparent symptom of the trouble. Refer to the equivalent symptom in the troubleshooting chart, note the probable trouble, and take the indicated corrective
action for each probable trouble. If the indicated corrective action does not restore the equipment to an operable condition, report the deficiency in accordance with prescribed station procedures. When a particular trouble symptom is observed, it can be corrected by repairing or replacing one or more of the components listed in the checks and corrective measures column. First check resistors, capacitors, relays, and other nonplug-in electrical or mechanical components before replacing the component. When a PC card trouble is suspected, check the PC card by substituting a new card. Always recheck the punched tape reader operation after repairs or replacements are performed.

4-10. Punched Tape Reader Troubleshooting Chart

| Item No. | Trouble symptom | Probable cause | Checks and corrective measures |
| :---: | :--- | :--- | :--- |
| 1 | Fan does not operate. | Blown fuse at power supply PS1. | Replace FAN fuse at front panel of power <br> supply. |
| 2 | Drive motor does not <br> operate. | Blown fuse at power supply PS1. | Replace DRIVE motor fuse at front panel <br> of power supply. |
| 3 | Indicator lamps do not <br> light. <br> Equipment shuts off or <br> cannot be turned on. | Blown fuse at power supply PS1. <br> Failure in one or more of the regula- <br> tors power supply PS1. | panel of power supply. fuses at front <br> Check for blown 120 VAC PWR SUP IN- <br> PUT fuse, or $-12 \mathrm{~V},+412 \mathrm{~V}$, or +4.75 |
|  |  | FAST BLO fuses at front panel of power <br> supply |  |


| Item No. | Trouble symptom | Probable cause | Checks and corrective measures |
| :---: | :---: | :---: | :---: |
| 5 | Excessive contact bounce. | a. Low contact force (less than minimum specified in fig. 4-23. <br> b. Improperly deflashed fixed contact. <br> c. Defective starwheel too loosely held by lever. <br> d. Switch timing incorrect (data holes not correctly phased with starwheels). <br> e. Tape drag high lover 345 grm- /inch on $2 \times 2$ paper/mylar/ paper sandwich tape).(Two all-hole characters, two nohole characters, in alternate fashion. Measured with capstan drive mechanism spider | a. Adjust fixed contact down and movable contact up to increase hole contact force para (4-48). <br> b. Replace fixed contact (paras 4-48, 4-49 and 4-51). <br> c. Replace starwheel lever assembly (para 435). <br> d. Adjust for correct switch timing as specified in para 4-52 <br> e. Correct as follows: <br> (1) Adjust read head contact (pare 4-49). <br> (2) Be sure that capstan and capstan shaft turn freely without binding or rubbing on adjacent parts. <br> (3) Measure capstan height (para 4-13). |

5.1 Intermittent, erratic, or no output from read head

Tape fails to advance.

Tape skips (advances two or more steps on one pulse).
Punched tape reader alarm conditions.
a. Inability to reset out of stop.
a. Low contact force (less than minimum specified in fig. 4-23.
b. Improperly deflashed fixed contact.
c. Defective starwheel too loosely held by lever.
d. Switch timing incorrect (data holes not correctly phased with starwheels).
e. Tape drag high lover 345 grm-/inch on $2 \times 2$ paper/mylar/ paper in alternate fashion. Measured with capstan drive mechanism spider gear removed and by pulling tape through closed tape holddown.)
a. Dirty contacts.
b. Defective read head.
a. Insufficient armature tip clearance.
b. Excessive heel gap.
c. Excessive spring tension.
d. Mechanical bind on capstan or shaft.
e. Slewing lever disengaged.
f. No solenoid drive pulse.
g. Alarm STOP condition present.
a. Excessive armature tip clearance.
b. Insufficient spring tension (fig. 4-27)
c. Broken or chipped escapement teeth.
a. One or more of following
(1) Alarm stop condition present.
(2) Operator alarm condition present.
a. Adjust fixed contact down and movable para (4-48).
b. Replace fixed contact (paras 4-48, 4-49 and 4-51).
c. Replace starwheel lever assembly (para 435).
d. Adjust for correct switch timing as specified in para 4-52
e. Correct as follows:
(1) Adjust read head contact (pare 4-49).
(2) Be sure that capstan and capstan shaft turn freely without binding or rubbing on
(3) Measure capstan height (para 4-13).
a. Check for waveshape as shown in figure 4-23.1. If improper, proceed as follows:
(1) Remove bottom cover (10 fig. 4-12) and tape deck assembly (para 4-32a).
(2) Clean contacts using freon bath (or equivalent solvent that will not deteriorate plastic), allow to dry and vacuum to remove any remaining particles of dirt.

## CAUTION

Take care not to bend contacts.
(3) Replace tape deck assembly. (para 432b) and bottom cover.
b. Replace read head (para 4-34).
a. Adjust armature tip clearance (para 4-59.
b. Adjust heel gap (para 4-58).
c. Adjust spring tension (para 4-57).
d. Correct as follows:
(1) Be sure that capstan and capstan shaft turn freely without binding or rubbing on adjacent parts.
(2) Measure capstan height (para 4-13).
e. Check slewing lever for possible disengagement. Re-arrange slewing lever.
f. Replace PC cards A1 (A66209), A14 (A65433), and A16 (A65429).
g. Check fault indicator and correct fault.
a. Adjust armature tip clearance (para 4-59.
b. Adjust spring tension (para4-57).
c. Replace friction clutch (para 4-39).
a. Proceed as follows:
(1) Check error indicators and correct fault.
(2) Check for tight tape condition.

## Change 7 4-4

$\left.\begin{array}{llll}\hline \text { Item No. } & \text { Trouble symptom } & \text { Probable cause } & \text { Checks and corrective measures } \\ \hline & & \text { (3) Defective PC card. } & \text { (3) } \begin{array}{l}\text { Replace PC cards A16 } \\ \text { (A65429) and A16 (A65437). }\end{array} \\ & & \text { Check OSC output on PC }\end{array}\right]$ card A1 (A65209).

## Change 6 4-4.1

| Item No. Trouble symptom | Probable cause | Checks and corrective measures |
| :---: | :---: | :---: |
| a. Invalid character | a. One or more of following: <br> (1) Improper character on tape <br> (2) Defective character decoding <br> (3) Defective PC card <br> (4) Failure to sense tape-out | a. Proceed as follows: <br> (1) Check tape for invalid character and correct tape if necessary. <br> (2) Replace PC card A6 (A665421). <br> (3) Replace PC card A15 (A65437). <br> (4) Replace PC card A7 (A66426). |

b. No or improper invalid character alarm with an invalid character
c Tight tape
d. Improper or no tight tape alarm with tight tape condition.
e. Tape out indication.
f. End of tape condition.
g. Improper or no tape out alarm with end of tape condition.
h. Improper or no cancel alarm with cancel condition present.
i. Motion fail indication.
b. One or more of following:
(1) Defective character decoding
(2) Defective alarm logic
(3) Defective lamp DS2
(4) Defective lamp driver
c One or more of following:
(1) Tight tape condition
(2) Defective tape microswitch.
(3) Defective alarm logic.
d. One or more of following:
(1) Defective microswitch.
(2) Defective alarm logic.
(3) Defective lamp DS6.
(4) Defective lamp driver.
(5) Tight tape sensing arm spring tension
e. One or more of following:
(1) Tape out condition.
(2) Defective alarm logic.
$f$. Defective tape out microswitch.
g. One or more of following:
(1) Defective alarm logic.
(2) Defective end of tape microswitch.
(3) Misaligned tape holddown comb assembly.
(4) Defective lamp DS6.
(5) Defective lamp driver.
h. One or more of following:
(1) Defective interface card.
(2) Defective alarm logic.
(3) Defective lamp DS2.
(4) Defective lamp driver.
i. One or more of following:
(1) Defective tape.
(2) Defective alarm logic.
(3) Defective timing.
(4) Motion sensor adj.
(5) Defective motion sensor.
(6) Defective motion sensor amplifier.
(7) Misaligned tape holddown.
(8) Defective friction clutch.
(9) Improper armature tip clearance. 4-59.
(10) Spring tension on armature tip.
a. Proceed as follows:
(1) Check tape for invalid character and correct tape if necessary.
(2) Replace PC card A6 (A665421)
(4) Replace PC card A7 (A66426).
b. Proceed as follows:
(1) Replace PC card A6 (A65421).
(2) Replace PC card A15 (A65437).
(3) Replace lamp.
(4) Replace PC card A3 (SM-E-546659).
c Proceed as follows:
(1) Check tape threading and clear tight tape condition.
(2) Replace microswitch.
(3) Replace PC card A16 (A66437).
d. Proceed as follows:
(1) Replace microswitch.
(2) Replace PC card A15 (A65437).
(3) Replace lamp.
(4) Replace PC card A3 (SM-D-546686).
(5) Check spring tension (para 4-46ج).
e. Proceed as follows:
(1) Check for torn tape.
(2) Replace PC card A16 (A665437).
f. Replace or reposition microswitch.
g. Correct as follows:
(1) Replace PC card A-15 (A65437).
(2) Replace microswitch.
(3) Check and realign comb assembly.
(4) Replace lamp.
(5) Replace PC card A3 (SM-D-5656).
h. Proceed as follows:
*(1) Replace PC card A4 65216).
(2) Replace PC card A16 (A665437).
(3) Replace lamp.
(4) Replace PC card A3 (SM-D-546656).
i. Proceed as follows:
(1) Check tape for torn sprocket holes.
(2) Replace PC card A16 (A65437n.
(3) Replace PC card A14 (A665433).
(4) Adjust motion sensor (para 4-60).
(5) Replace card lamp or card sensor in motion sensor assembly (para 4-33).
(6) Replace amplifier in reader mechanism (para 4-36.
(7) Check for proper clearance.
(8) Check for broken or worn teeth and replace (pare 4-39).
(9) Check tip clearance and adjust para
(10) Check spring tension and adjust (pare 4-57).

| Item No. | Trouble symptom |
| :---: | :---: |
|  | j. No or improper motion fail indication with motion fail (A65433). condition <br> k. No local test mode or indication. (A65429). |
|  | I. No feed mode or indication. |
|  | m. No pilot header or indication.(1) Defectiv |
|  | n. No assigned mode indication. <br> (A65216). |
|  | o. No high speed mode or low speed mode indication |
| 10 | Data or transmission trouble. <br> a. Punched tape reader fails to transmit ready (start fails to turn green). |


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| :---: | :---: | :---: | :---: |
| Item No. | Trouble symptom <br> b. Punched tape reader fails to be selected (start fails to turn white).*** <br> c. Punched tape reader fails to step to first nonidle message character <br> d. Read error in ASCII.*** | b. One or more of following: <br> (1) Defective interface receiver <br> (2) Defective control logic <br> (3) Defective lamp driver <br> (4) Defective lamp Z7. | b. Proceed as follows: <br> *(1) Replace PC card A4 (A65215). <br> (2) Replace PC card A16 (A65429). <br> (3) Replace PC card A3 (SM-D-546656). <br> (4) Replace lamp. |
|  |  | c. One or more of following: <br> (1) Tape handling <br> (2) Continuous step <br> (3) Defective control logic <br> d. One or more of following: <br> (1) Defective input register <br> (2) Incorrect read head timing | c. Proceed as follows: <br> (1) Check for proper tape loading. <br> (2) Replace PC card A15 (A65437). <br> (3) Replace PC card A16 (A65429). <br> d. Proceed as follows: <br> (1) Replace PC card A7 (A65425). <br> (2) Check data bit switching for correct timing and minimum switching noise Adjust timing if necessary. <br> (3) Check to verify correct mode. |
|  |  |  |  |
|  |  | (3) Improperly set ASCII/ ITA-2 switch. |  |
|  |  | (4) Defective polar interface | **(4) Replace PC card A5 (A65205). |
|  |  | (5) Timing generator | (5) Replace PC card A14 (A65433) |
|  | e. Read error in ITA mode.*** | e. One or more of following:(1) Improperly set ASCII/ITA-2 switch.(2) Defective input register(3) ITA cede converter input(4) Defective decode matrix(5) Defective encode matrix(6) Defective decode matrix(7) Defective encode matrix(8) ASCII code converter out(9) put.(9) Defective polar interface. | e. Proceed as follows: <br> (1) Check to verify correct mode. |
|  |  |  | (2) Replace PC card A7 (A65425). |
|  |  |  | (3) Replace PC card A8 (A53418). |
|  |  |  | (4) Replace PC card A9 (A53725). |
|  |  |  | (5) Replace PC card A10 (A53721). |
|  |  |  | (6) Replace PC card All (A53725). |
|  |  |  | (7) Replace PC card A12 (A53721). |
|  |  |  | (8) Replace PC card A13 (A53434). |
|  |  |  | ${ }^{* *}$ (9) Replace PC card A5 (A65205). |
|  | f. Parity error at CCU.*** | $f$. One or more of following: <br> (1) Defective input register. <br> (2) Defective polar interface. <br> (3) Incorrect read head timing | f. Proceed as follows: <br> (1) Replace PC card A7 (A65425-001). <br> **(2) Replace PC card A5 (A65205-001). <br> (3) Check data bit switching for correct timing and minimum switching noise. Adjust timing if necessary. |
|  | g. No data transmission to CCU when selected.*** | (4) Bad parity on ASCII tape. <br> g. One or more of the following: <br> (1) Defective timing <br> (2) Defective control logic <br> (3) Defective receiver <br> (4) Defective transmitter | (4) Check tape and replace if necessary. <br> g. Proceed as follows: <br> (1) Replace PC card A14(A65433). <br> (2) Replace PC card A16 (A65429). <br> *(3) Replace PC card A4(A65215). <br> **(4) Replace PC card A5(A65205). |
| 11 | Irregular or no capstan drive mechanism operation. | a. Binding or broken gears. <br> b. Defective drive belt <br> c. Defective friction clutch <br> d. Defective drive motor | a. Check gear drive train and replace any defective gears (para 4-39). <br> b. Replace broken drive belt. <br> c. Replace clutch (para 4-39). <br> d. Check for drive motor operation and replace if necessary (para 4-40. |

## NOTES

*PC cards No. A65215 and A65223 are interchangeable.
**PC cards No, A65205 and A65227 are interchangeable.
***Supplemental data is provided ir paragraph 4-10.1 for punched tape readers that have been modified by the addition of a TIG assembly.

## Change 4 4-7

## 4-10.1 Punched Tape Reader/Transmission Identification Generator Troubleshooting Chart

The trouble symptoms listed under item 10 of the following troubleshooting chart are supplemental items to data provided in paragraph 4-10 above. The trouble symptoms listed in items 12 through 14 are applicable only to the TIG assembly operation. To troubleshoot a punched tape reader having been modified by the addition of a TIG assembly, refer to the troubleshooting charts in both paragraph 4-10 and this paragraph.(NOTE: In many instances, defective read heads (especially on those assemblies having intermittent or erratic outputs) can be repaired by cleaning of contacts)

| Item No. | Trouble symptom |
| :--- | :--- |
| 10 | b.Punch tape reader <br> fails to he selected <br> (start fails to turn <br> white). <br> d.Read error in <br> ASCII. <br> e. Read error in ITA <br> mode. <br> f.Parity error at <br> CCU. <br> g.No data transmission <br> to CCU when se- <br> lected. <br> a. Improper TIG mode <br> or indication. <br> (TIG on lamp fails <br> to turn white). |
| Transmission identifica- <br> tion sequence trouble. <br> a. No data transmis- <br> sion |  |
| b. Improper data trans- |  |
| mission. |  |

mission.
a. One or more of the following:
(1) Defective TIC control logic.
(2) Defective interface transmitter or receiver.A65223).
(3) Defective alarm logic $\qquad$
(4) Defective punched tape reader control logic.
b. One or more of following:
(1) Defective TIG control logic.
(2) Defective oscillator $\qquad$
(3) Defective neutral interface.
(4) Defective polar interface
(5) Defective alarm logic- $\qquad$
Sequence counter trouble.
a. Counter cannot be manually loaded.
(6) Defective TIG control logic.
(10) Defective TIG control logic.
(5) Defective TIG control logic.
(5) Defective TIG control logic.
a. One or m-re of the following:
(1) Defective TIG control logic.
(2) Defective switch A7S1 $\qquad$
$\qquad$
(3) Defective lamp A7DS
a. Processed as follows.
(1) Replace PC card A2 (12-980081).
(2) Replace switch A7S1.
(3) Replace lamp A7DS1
a. Proceed as follows:
(1) Replace PC card A2 (12-890081).
(2) Replace PC card A4 (Afi5215 or
(3) Replace PC card A15 (A65437).
(4) Replace PC card A16 (A65429).
b. Proceed as follows:
(1) Replace PC card A2 (12-890081).
(2) Replace PC card A1 (AP5209).
(3) Replace PC card A4 (A65215 or A69.223).
(4) Replace PC card A5 (A65205 or A65227).
(5) Replace PC card A15 (A65437).
a. Proceed as follows:
(1) Replace counter module A7A1Z1.
(2) Replace counter module A7A1Z2.
(3) Replace counter module A7AIZ3.
(4) Replace display module A7AID-S2U.
(5) Replace display module A7A1-DS2T.
(6) Replace display module A7A1D-S2H
(7) Replace switch A7S2U.
(8) Replace switch A7S2T.


## 4-11. Power Supply Troubleshooting Procedure

a. If there is any malfunction in any of the regulated supplies in the power supply the sequence module A12, in this supply automatically shuts down the entire supply. In order to troubleshoot the power supply, the sequence module must be removed and in its place a manual control card (Saratoga Industries part No. 39245)
[fig. 5-22], must be installed. This control card contains manually operated switches which permit the regulated supplies to be turned on one at a time. 7
b. In order to use the manual control card to troubleshoot the power supply, first operate all the SR switches of the manual control card in the following sequence: $-12 \mathrm{v},+4.75 \mathrm{v},+12 \mathrm{~V}$, and +48 v . This should turn on all the regulated supplies, which can be monitored at the test jacks

## $\rightarrow$ WARNING

120 VAC is present on Power Supply PS1 (and PS2 in Dual Paper Tape Readers) Sequencer PC Card A12. Do not remove PC Card PS1A12 prior to removing AC voltage to the Punched Tape Reader from the AC power source.
at the front of the power supply, as described in paragraph 463 (which describes the adjustment procedure for the regulated supplies). If the regulated supplies all go on and are providing outputs within 90 percent of rated value the malfunction was in the sequence module A12. If the output voltage of one (or more) of the regulated supplies does not meet the required specification, the voltage regulator, or its associated rectifier-filter network is defective, as summarized in the chart in e below. If all regulated supplies are not operating the ac power transformer (A9T1) is defective or a front panel ac fuse is blown.
c. If it is suspected that there may be ripple in the output voltage of any one of the regulated
supplies, connect an oscilloscope to the output test jacks at the front of the power supply normally monitored by means of a digital voltmeter (para 463). The ac ripple should not exceed the following peak-to-peak values:

Test point monitored
Test points Maximum ripple (volts, peak to peak)
+4.75 and COM......................... 0.012

+ 12 and COM........................... 0.02
-12 and COM.............................. 0.02
-48 and COM............................. 0.02
d. If one of the power supplies is completely off, check the front panel fuse associated with this supply. If the fuse is $n$, defective, the cause of trouble is in the corresponding voltage regulator card specified in the troubleshooting chart in e below.
e. Refer to the following chart to locate troubles in the power supply:

| Item No. | Trouble symptom | Probable cause | Checks and corrective measures |
| :---: | :---: | :---: | :---: |
| 1 | Power supply shuts off but can be made to operate when manual control card is installed. | Sequence module PS1A12 defective | Replace module PS1A12. |
| 2 | +4.75 -volt output out of tolerance. | a. Incorrectly adjusted +4.75 -volt regulator. <br> b. Defective +4.75 -volt regulator <br> c. Defective rectifier-filter network. | a. Adjust +4.75 -volt regulator as described in paragraph 4-63. <br> b. Replace module PS1A1. <br> c. Replace heatsink component assembly PS1A4. |
| 3 | +12-volt output out of tolerance. | a. Incorrectlyadjusted+12-volt regulator. <br> b. Defective +12 -volt regulator <br> c. Defective rectifier-filter network. | a. Adjust +12 -volt regulator as described in paragraph 4-63. <br> b. Replace module PS1A2. <br> c. Replace heatsink component assembly PS1AS. |
| 4 | -12-volt output out of tolerance. | a. Incorrectly adjusted -12-volt regulator. <br> b. Defective -12-volt regulator <br> c. Defective rectifier-filter network. | a. Adjust -12-volt regulator as described in paragraph 4-63. <br> b. Replace module PS1A2. <br> c. Replace heatsink component assembly PS1A5.. |
| 5 | -48-volt output out of tolerance. | a. Incorrectly adjusted-48-volt regulator. <br> b. Defective -48 -volt regulator <br> c. Defective rectifier-filter network. | a. Adjust -48 -volt regulator as described in paragraph 4-63. <br> b. Replace module PS1A3 or PS1A6. <br> c. Replace heatsink component assembly PS1A4. |
| 6 | Excessive ripple in regulated dc outputs: |  |  |
|  | a. +4.75 -volt output $\qquad$ <br> b. +12 -volt output $\qquad$ | a. Defective filter capacitor A9C2 or A9C3. | a. Replace filter capacitor(s). |
|  | c. -12-volt output ........... | b. Defective filter capacitor A9C4 ...... | b. Replace filter capacitor. |
|  | d. -48-volt output .......... | c. Defective filter capacitor A9C5 ...... <br> d. Defective filter capacitor A9C6 ...... | c. Replace filter capacitor. <br> d. Replace defective filter capacitor. |

Note. The supplementary troubleshooting information in blaragraphs 4-12|through 4-15 is provided to permit restoration of the punched tape reader to normal performance when no adjustments can be made to correct the deficiency.

## 4-12. Friction Clutch Torque Measurement

Note. Operate the motor of the punched tape reader for at least 5 minutes prior to performing this procedure because the friction clutch must be at operating temperature to obtain an accurate torque measurement.
a. Attach the torque arm 226620 to the idler shaft and the 100-to-00-gram gage to the torque arm as shown in figure 4-2. Check the friction clutch torque as follows:
(1) Operate the motor, but do not pulse the reader.
(2) Carefully pull the upper end of the torque arm in the direction shown and note the gage indication when the escapement tooth is moved slightly away from the armature actuator tip.

Allow the torque arm to return slightly and note the gram gage indication before the escapement tooth comes in contact with the armature actuator tip. The sum of the two indications read must be between 250 and 300 grams.
b. If the friction clutch torque is not between 250 and 300 grams, replace the friction clutch. (25 thru 30, fia. 4-16) as described in paragraphs 4-38 and 4-39.


Figure 4-2. Friction clutch torque measurement.

## 4-13. Capstan Height Measurement

Remove tape deck assembly (47, fig. 4-12) as described in paragraph 4-32. Mount capstan height gage 375560 on the read head with screws (46, fig. 412) as shown in figure 4-3
a. Requirement. The capstan rim (not the teeth) must be flush with the top of gage.
b. Adjustment. Loosen the two read head
mounting screws (52, fig. 4-12) and sight along top of gage. Move read head up or down, as required. Tighten read head mounting screws. If correct capstan height cannot be obtained with this adjustment, replace the read head (64,fig. 4-12), adapter plate (2.fig. 4-16), or capstan shaft (31, fig. 4-16), as required.


Figure 4-3. Capstan height measurement.

## 4-14.Tape Pull Measurement

a. Insert a short length of paper tape having sprocket holes punched into the reader mech.
b. Hook gram gage 4043402 to the end of the tape.
c. Pulse the armature at a slow rate to release the escapement and observe the gage indication
when the tape stalls. The gage should indicate a force of at least 450 grams.
d. If the gage indication is not at least 450 grams check for free rotation of the capstan shaft by turning SLEW lever to the left, then turning shaft by hand. If the shaft does not turn freely, remove the capstan drive mechanism assembly (para 4-38), and reposition adapter plate (2 fig. 4-16) to realign the shaft. If the shaft does rotate freely, and the force in $\underline{\mathbf{c}}$ above is still under 450 grams, replace the friction clutch (para 438 and 4-39).

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## 4-15. Troubleshooting Reference Data

a. Coil and Frame Assembly Voltage. The voltage rating of the coil in the coil and frame assembly ( 51, fig. 4-16) is 48 volts.
b. Relay K1 Resistance. The resistance of relay K1 is 72 ( $\pm 10$ percent) ohms. Relay K1 is used only with units containing two tape readers.
c. Transformer PSIA9TI. Proper resistance for PS1A9T1 are as follows:

| Winding terminals | Maximum resistance (ohms) |
| :---: | :---: |
| $1-2$ | 0.270 |
| $3-7$ | 0.270 |
| $4-7$ | 0.021 |
| $5-7$ | 0.048 |
| $6-7$ | 0.011 |
| $7-8$ | 0.011 |
| $7-9$ | 0.048 |


| Winding terminals | Maximum resis tance (ohms) |
| :---: | :---: |
| $7-10$ | 0.021 |
| $7-11$ | 0.270 |
| $12-13$ | 0.510 |

d. Transformer PS1A12T1 Winding Resistances. The winding resistances of transformer PS1A12T1 are listed below.

| Winding terminals | Maximum resistance (ohms) (+ 15 percent) |
| :---: | :---: |
| 1-6 | 1.250 |
| 2-4 | $0 ., 90$ |
| 3-5 | 0.370 |
| Additional Refer | ce Data. Refer to the |
| interconnection and schematic diagrams (figs. 8-1 through 8-23) for detailed circuitry information when troubleshooting the punched tape reader. |  |
|  |  |
|  |  |

## Section IV. REMOVAL AND REPLACEMENT

## 4-16. General

The following paragraphs describe the removal and replacement of major assemblies, subassemblies, and components of the punched tape reader. These paragraphs also describe the disassembly and reassembly of major assemblies and subassemblies when not in the order of index numbers on exploded views or when special tools and procedures are required. Use these procedures in conjunction with the troubleshooting, lubrication, repair, and adjustment procedures described in paragraphs 4-9 through 4-15, 48, 4-45, .and 4-62, respectively.
a. Removal and Disassembly.
(1) Disassemble the punched tape reader only to the extent necessary to inspect, clean, lubricate, and replace a defective part, or to adjust the assembly that is in need of maintenance.
(2) When removing shims, note the number and thickness of 'shims used at each point. Be sure to replace the same thickness of shims at each point (unless otherwise specified) when reassembling the assembly.
(3) When removing springs that are very similar in appearance, tag or otherwise identify each spring to insure proper identification during reassembly.
b. Reassembly and Replacement.
(1) Inspect all removed parts for evidence of excessive wear or damage. Install only parts that are unquestionably serviceable.
(2) Apply a coat of antiseize compound to all steel screws that are installed in aluminum castings.
(3) Check to be sure that mating gears and me-chanical linkages are properly engaged before tightening the mounting screws or nuts.

## CAUTION

When securing parts in place, be careful not to tighten the mounting screws or nuts excessively.
(4) Apply sealing compound (SM-B-583244008) to the areas indicated by the note on figure 4-5.
c. Post Replacement Checks. After replacing a past or an assembly, perform the operation checkout procedures given in section Ill of Chapter 2.

## NOTE

A quick and efficient method of repairing loose or stripped cabinet frame back panel nuts is to install a floating nut, NSN 5310-00-864-5274, P/N FZ9589-31 , in its place.

## 4-17. Removal and Replacement of Control Panel Assemblies A3 and A6

a. Removal. Remove the eight screws (1, fig. 4-5), flat washers (2), and lockwashers (3), and separate control panel assemblies (4 and 5) from reader inclosure (27).

NOTE
At this point, the attaching cables are still clamped to the enclosure. To completely remove the front panel, the cables connecting to power supply PS1 and logic assembly A1 must be removed. This is not necessary for replacement of front panel components, however.
b. Replacement. To replace control panel assemblies ( 4 and 5 , fig. 4- $\xi$ ), reverse the removal procedure in a above.


Figure 4-5. Punched tape reader, component location diagram.
(Sheet 1 of 4).

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Figure 4-5. Punched tape reader, component location diagram. (Sheet 2 of 4)


Figure 4-5. Punched tape reader, component location diagram. (Sheet 3 of 4)

TH 74 40-219-45-24 (4)

| 1 | Screw panhead, No. 8-82, 7/16 in. long |
| :---: | :---: |
| 2 | Washer, fat, No. 8 |
| 3 | Lockwasher, No. 8 |
| 4 | Control panel assembly (As) |
| 5 | Control panel assembly (A6) ${ }^{\text {a }}$ Blank panel ${ }^{\text {b }}$ |
| 5.1 | Nut, hex, No. 10-32 |
| 5.2 | Screw, panhead, No. 10-32, 8/4 in. long ' |
| 5.3 | Lockwasher, No. $10^{\text {b }}$ |
| 5.4 | Washer, flat, No. $10^{\text {b }}$ |
| 6 | Reader mechanism assembly (A2) |
| 6.1 | Reader mechanism assembly (A5) ${ }^{\text {a }}$ Tape clip panel ${ }^{\text {b }}$ |
| 7 | Screw, panhead, No. 8-32, 1/2 in. long |
| 8 | Washer, flat, No. 8 |
| 9 | Lockwasher, No. 8 |
| 10 | Logic assembly (A1, A4) |
| 11 | Interface plate assembly |
| 12 | Interface plate assembly |
| 13 | Power supply (PSI, PS2) |
| 14 | Screw, hex head, No. 10-32 |
| 15 | Washer, flat, No. 10 |
| 16 | Lockwasher, No. 10 |
| 17 | Slide |
| 18 | Screw, panhead, No. 10-32 |
| 19 | Lockwasher. No 10 |
| 20 | Shield assembly |
| 21 | Filter assembly (FL1) |
| 22 | Screw, panhead, No. 8-32, 7/16 in. |
| 23 | Washer, flat, No. 8 |
| 24 | Lockwasher, No. 8 |
| 24.1 | Screw, panhead, No. 10-32, $1 / 2 \mathrm{in}$. long |
| 24.2 | Washer, flat, No. 10 |
| 243 | Lockwasher No. 10 |
| 24.4 | Relay and filter assembly |
| 25 | Grill assembly |
| 25.1 | Stud |
| 25.2 | Nut, self-locking |
| 25.3 | Grill |
| 26 | Blower (B1) |
| 26.1 | Capacitor |
| 262 | Clockwise blower wheel |
| 26.3 | Counter-clockwise blower wheel |
| 26.4 | Blower motor |
| 26.6 | Filter, |
| 20.1 | Standoff |

Figure $4-5{ }^{4)}$ Punched tape reader, component location diagram (sheet 4 of 4).

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126 Lockwasher, external tooth, No.
130
No. 8
127 Nut, hex, No. 10-32
128 Lockwasher, No. 10
129 Washer, flat, No. 10

Cable bar clamp
Nut, hex, No. 8-32 Lockwasher, No. 8 Washer, flat, No. 8

4-18. Disassembly and Reassembly of Control Panel Assemblies A3 and A6
(fig. 4-6
a. Disassembly. Disassemble control panel
semblies (4 and 5,fig3. ${ }^{4-5}$ ) by following the sequence of index numbers' in figure 4-6.
b. Reassembly. To reassemble control panel assemblies (4 and 5 fig. 4-5), reverse the disassembly procedure in a above.


| 1 | Push switch (Z7) |
| :--- | :--- |
| 2 | Push switch (Z8) |
| 3 | Push switch (Z2) |
| 4 | Push switch (Z4) |
| 5 | Push switch (Z1) |
| 6 | Push switch (Z6) |
| 7 | Push switch (Z5) |
| 8 | Push switch (Z9) |
| 9 | Push switch (Z3) |


| 10 | Indicator light (DS1) |
| :--- | :--- |
| 11 | Indicator light (DS3) |
| 12 | Indicator light (DS2) |
| 13 | Indicator light (DS7) |
| 14 | Indicator light (DS4) |
| 15 | Indicator light (DS6) |
| 16 | Indicator light (DS5) |
| 17 | Lamp |
| 18 | Control panel |


| 19 | Nut, hex, No. 10-32 |
| :--- | :--- |
| 20 | Lockwasher, No. 10 |
| 21 | Washer, flat, No 10 |
| 22 | Cable clamp |
| 23 | Terminal lug |
| 24 | Terminal lug |
| 25 | Jumper |

Figure 4-6. Control panel assembly, component location diagram.

## 4-19. Removal and Replacement of Reader Mechanism Assemblies A2 and AS

a. Removal. Remove the reader mechanism assemblies ( 6 and 6.1 fig 4-5) as follows:
(1) Pull the two fastener handles on the mechanism assembly panel so that the handles extend straight out.
(2) Rotate the fastener handles $90^{\circ}$ to release the fasteners.
(3) Grasp the handles and pull the assembly out on its slides until the slides lock in place.
(4) Disconnect the two connectors at the rear of the assembly.
(5) Depress the slide stop catches on the left and right slide assemblies.
(6) Remove the assembly from the inclosure.
b. Replacement. To replace the reader mechanism assemblies ( 6 and 6.1 fig. 4-5), reverse the removal procedure in a above.

4-20. Disassembly and Reassembly of Reader Mechanism Assemblies A2 and A5
(fig. 4-7)
a. Disassembly. Disassemble the reader mech-
anism assemblies ( 6 and 6.1 , fig. 4-5) by following the sequence of index numbers in figure 4-7.
b. Reassembly. To reassemble the reader mechanism assemblies, reverse the disassembly procedure in a above.

Change 4 4-20


Figure 4-7. Punched tape reader mechanism assembly, component location diagram.

[^1]5 Panel fastener handle
6 Screw, panhead, 10-32, 5/8 in. long
7 Lockwasher, No. 10

9 Slide
10 Reader chassis
11 Reader mechanism assembly (A2)

## 4-21. Removal and Replacement of Logic

 Assemblies AI and A4a. Removal. Remove logic assemblies (10,fig. 4-5) as follows:
(1) Open the front doors of the enclosure.
(2) Release the panel fasteners by rotating the knobs until the arrow is vertical.
(3) Slide the logic assembly forward until the slides lock in place.
(4) Remove the four interface connectors which mate with J1 through J4.
(5) Remove the wires attached to the A sides of terminal blocks TB2 and TB3.
(6) Remove the four individual cable clamps located adjacent to TB2.
(7) Remove the bar clamp (2 nuts, washers, and lockwashers) which holds the cables to the
rear surface of the logic assembly. All connecting cables are now free from the logic assembly.
(8) Depress the slide stop catches (located midway along each of the top and bottom slide assemblies) and remove the logic assembly from the inclosure.
b. Replacement. To replace logic assemblies (10, fig. 4-5), reverse the removal procedure in a above.

## 4-22. Disassembly and Reassembly of Logic Assemblies A1, A4 <br> (fig. 4-8)

a. Disassembly. Disassemble logic assemblies (10 fig. 4-5) by following the sequence of index numbers in figure 4-8.
b. Reassembly. To reassemble logic assemblies (10, fig. 4-5), reverse the disassembly procedure in a above.

| 1 | PC card Al (No. A65209) |
| ---: | :--- |
| 2 | PC card A3 (No. SM-E-546659) |
| 3 | PC card A4 (No. A65215) |
| 3.1 | PC card A4 (No. A65223) |
|  | See note 1) |
| 4 | PC card A5 (No. A65205) |
|  | (See note 2) |
| 4.1 | PC card A5 (No A65227) |
|  | (See note 2) |
| 5 | PC card Afi (No A65421) |
| 6 | PC card A7 (No. AF5425) |
| 7 | PC card A8 (No. A53418) |
| 8 | PC card A9 All (No A53725) |
| 9 | PC card A10, A12 (No. A53721) |
| 10 | PC card A13 (No. A53434) |
| 11 | PC card A14 (No. A65433) |
| 12 | PC card A15 (No. A65437) |
| 13 | PC card A16 (No. A65429) |
| 14 | Pin identification overlay |
| 15 | Panel latch |
| 15.1 | Washer, flat, No. 12 |
| 16 | Push switch S1 (RESET) |
| 17 | Toggle switch S2 (ASCII-ITA- |
| 18 | 2 CODE SELECT) |
| 18 | Toggle switch guard |
| 19 | Screw, panhead, 10-32, 3,'4 |
| 20 | in. Ig. |
| 21 | Lockwasher, No. 10 |
| Washer, flat, No. 10 |  |


| 22 | Bow handle |
| :--- | :--- |
| 23 | Front panel |
| 23.1 | Panel assembly |
| 24 | Screw, panhead, 8-32, 3.'4 |
|  | in Ig. |
| 25 | Lockwasher. No. 8 |
| 26 | Nut, hex., No. 8-32 |
| 27 | Washer. fiat, No. 8 |
| 28 | Terminal block (TB2) |
| 29 | Marker strip |
| 30 | Screw, panhead, 6-32, 7/8 |
|  | in. Ig. |
| 31 | Lockwasher. No 6 |
| 32 | Nut. hex.. No. 6-32 |
| 33 | Washer. flat, No. 6 |
| 34 | Terminal block, (TB3) |
| 35 | Marker strip |
| 36 | Screw, panhead, 10-32, 5/8 |
|  | in. Ig. |
| 37 | Lockwasher, No. 10 |
| 38 | Nut. hex.. No. 10-32 |
| 39 | Washer, flat, No. 10 |
| 40 | Contact plate |
| 401 | Contact plate assembly |
| 40.2 | Screw, panhead, 6-32, 5,;16 |
| in. Ig. |  |
| 40.3 | PC card insulator |
| 40.4 | PC card electrical contact |
| 405 | Connector insulator |
| 40.6 | Contact pin (A1J1, A4J1) |

Figure 4-8-Continued.
40.7 Contact pin (AlJ2, A4J2)
40.8 Contact pin (A1J3, A4J3)

409 Contact pin (A1J4, A4J4)
41 Screw, nylon, 6-32, 1 '2 in. Ig.
42 Nut, hex., nylon, 6-32
43 Laminated bus (TBI)
431 Insulating strip
44 Screw, panhead, 6-32, 3/8 in Ig.
45 Lockwasher, No. 6
46 Washer, flat, No. 6
47 Spacer
48 Terminal lug
49 Screw, panhead, 10-32, 1/2
in Ig.
50 Nut, hex, No 10-32
51 Lockwasher, No. 10
52 Washer, flat, No. 10
52.1 Rubber grommet
52.2 Plastic trim
52.3 Screw, panhead, No. 10-32,
$1 / 2 \mathrm{in}$. Ig.
52.4 Nut, hex, No 10-32

525 Lockwasher, No 10
526 Washer, flat, No. 10
53 Slide
54 Chassis
55 Logic chassis assembly
5, Chassis assembly
$57 \quad$ Wiring harness
58 Terminal lug


NOTES: A
PC cards A65215 and A65223 are interchangeable in the A4 position. PC cards A65205 and A65227 are interchangeable in the A5 position. 3. PC card A2 and its associated connector are used only in punched tape readers that have been converted to include a Transmission Identification Generator (TIG) assembly.

Figure 4-8. Logic assembly, component location diagram.
Change 6 4-23

## 4-23. Removal and Replacement of Interface Plate

 Assembliesa. Removal. Remove interface plate assemblies (11 and 12 fig. 4-5) as follows:
(1) Remove ac power from the punched tape reader.
(2) Open the front doors of the reader inclosure.
(3) Remove the logic assembly from the reader as described in paragraph 4-21
(4) Remove the interface cable to the CCU from terminal strips TB1, TB2, and TB3 (or TB4, TB5, and TB6, as the case may be).
(5) Remove the two heavy brown wires from terminals 1 and 2 of TB3 (or TB6).
(6) Remove cable clamps fastening cables to the interface plate.
(7) Remove the four screws which fasten the interface plate to the enclosure. (8) Remove the interface plate with hanging cable through the entrance area vacated by the logic assembly.
b. Replacement. To replace the interface plate assemblies (11 and 12. fig. 4-5), reverse the removal procedure in a above.
4-24. Disassembly and Reassembly of Interface Assemblies
a. Disassembly. Disassemble interface plate assemblies (11 and 12 fig. 4-5) by following the sequence of index numbers in figure 4-9.
b. Reassembly. To reassemble interface plate assemblies, reverse the disassembly procedure in $a$ above.


Figure 4-9. Interface plate assembly, component location diagram.

4-25. Removal and Replacement of Power Supplies PS1 and PS2
Warning. Two persons are required for removal of the power supplies ( 13 fig. 4-5) from the reader inclosure (27). Use extreme care in handling the power supplies (13), to avoid injury to personnel or damage to equipment; no good grasping areas are present in the rear of these units.
a. Removal. Remove the power supplies (13,fig. 4-5) as follows:
(1) Remove ac power from the punched tape reader.
(2) Open the front doors of the inclosure.
(3) Rotate the two fastener knobs until the arrows are vertical.
(4) Use the two handles to pull the power supply out on its slides until the slides lock in. place.
(5) Remove the external cables from terminal boards TB1 and TB2.
(6) Remove the cable clamp at the rear of the power supply.
(7) Depress the slide stop catches on the left and right slide assemblies. Pull the power supply off the slides.
b. Replacement. To replace the power supplies, reverse the removal procedure in a above.
c. Removal of Power Supply PS-1 for Troubleshooting and Repair.

## CAUTION

Power unit weighs 70 pounds. This
procedure should never be undertaken by less than two persons.
(1) Open the circuit breaker supplying power to the equipment. Even with the unit AC POWER switch in the OFF position, 120 VAC is present at the power supply.
(2) Depress the power supply assembly slide latches and pull the power supply out to the stops on the slide.
(3) Remove the cable clamp on the rear of the power supply which secures the cables connected to the power supply assembly.
(4) Depress the power supply slide latches and pull the power supply forward until it is free of the slide.
(5) Rotate the power supply assembly 1800 in a counter-clockwise direction so the bottom of the chassis is facing up.
(6) Replace the power supply in the slides. Close the power supply far enough to enable the slides to support the assembly. Power can now be applied and the necessary maintenance performed.
(7) To restore the power supply to its operating position, insure the circuit breaker supplying power to the unit is OFF, then reverse the procedures in (1) through (6) above.

## NOTE

When reinstalling the power supply to the operating position, always rotate power supply in a clockwise direction back to the upright position to prevent twisting the power cables.
4-26. Disassembly and Reassembly of Power Supplies PSI and PS2
Disassemble the power supply in the order of index numbers in figure 4-10. Assemble the power supply in the reverse order of index numbers.

Caution: When replacing semiconductor components of heat sink subassemblies A4 (fig. 518), A5 (fiq. 5-19), or A6 (fig. 5-20), clean mating surfaces of semi-conductor and heat sink chassis and apply a light coat of Dow Corning DC340 silicone grease to mating surfaces before mounting the semiconductor.


Figure 4-10. Power supply component location diagram.

## LEGEND FOR FIGURE 4-10:

| 1 | Screw, hex head, No. 8-32, 3/8 in. long |
| :---: | :---: |
| 2 | Lockwasher, No. 8 |
| 3 | Washer, flat, No. 8 |
| 4 | Front panel assembly (A10) |
| 4.1 | Front panel |
| 5 | Latch |
| 5.1 | Washer, flat, No. 12 |
| 6 | Fuse holder (XF1) |
| 7 | Fuse holder (XF4) |
| 8 | Fuse holder (XF2, XF3, XF9, XF10) |
| 9 | Fuse holder (XF5, XF7, XF9) |
| 10 | Fuse holder (spare) |
| 11 | Fuse, 10 amp , slow blow (F5, F8 and spare) |
| 12 | Fuse, 3 amp, slow blow (F7, F9, F10 and spare) |
| 13 | Fuse, 15 amp , fast blow (F1 and spare) |
| 14 | Fuse, 10 amp , fast blow (F2, F3, F4 and spare) |
| 15 | Screw, hexhead, No. 10-32, 5/8 in. long |
| 16 | Lockwasher, No. 10 |
| 17 | Washer, flat, No. 10 |
| 18 | Handle |
| 19 | Test point jack (TP2 thru TP5) |
| 20 | Test point jack (TP1) |
| 21 | Screw, hexhead, No. 6-32, 3/8 in. long |
| 22 | Lockwasher, No. 6 |
| 23 | Washer, flat, No. 6 |
| 24 | Fuse cover |
| 25 | Screw, flathead, No. 6-32, 5/16 in. long |
| 26 | Side plate, left hand |
| 27 | Side plate, right hand |
| 28 | Screw, hexhead, No. 8-32, 3/8 in. long |
| 29 | Lockwasher, No. 8 |
| 30 | Washer, fiat, No. 8 |
| 31 | Sequence module bracket, left hand |
| 32 | Sequence module bracket, right hand |
| 33 | Card guide |
| 34 | Screw, hexhead, No. 4-40, $1 / \mathrm{in}$. long |
| 35 | Lockwasher, No. 4 |
| 36 | Washer, flat, No. 4 |
| 37 | Nut, hex. No. 4-40 |
| 38 | Polarization key |
| 39 | Electrical receptacle connector (A9J4) |
| 40 | Sequence module component board assembly (A12) |
| 41 | Screw, hexhead, No. 10-32, 4-7/8 in. long |
| 42 | Screw, hexhead, No. 10-32, 6-3/8 in. long |
| 43 | Lockwasher, No. 10 |
| 44 | Washer, fiat, No. 10 |
| 45 | Capacitor nest |
| 45.1 | Insulator |
| 46 | Capacitor, 82,000 of, 15 vdc (A9C2, A9C3) |
| 47 | Capacitor, 44,000 Of, 25 vdc (A9C4, A9C5) |
| 48 | Capacitor, 6700 uf, 100 vdc (A9C6) |
| 49 | Capacitor, 1500 of, 75 vdc (A9C1) |
| 50 | Screw, hexhead, No. 6-32, 5/8 in. long |
| 51 | Washer, flat, No. 6 |
| 52 | Lockwasher, No. 6 |
| 53 | Nut, hex, No. 6-32 |
| 54 | Screw, hexhead, No. 6-32, 3/8 in. long |
| 55 | Capacitor, 9200 of, 10 vdc (A9C7, A9C11) |
| 56 | Capacitor, $4600 \mu 20$ vdc (A9C8, A9C9) |
| 57 | Capacitor, $1200 \mu \mathrm{f}, 75 \mathrm{vdc}$ (A9C10) |
| 58 | Capacitor bracket |
| 59 | Screw, hexhead, No. 6-32, 3/8 in. long |
| 60 | Lockwasher, No. 6 |
| 61 | Washer, flat, No. 6 |
| 62 | Heatsink assembly (All) |
| 62.1 | Endplate |
| 62.2 | Screw, panhead, No. 6-32, 1/2 in. long |
| 62.3 | Lockwasher, No. 6 |

Screw, hex head, No. 8-32, 3/8 in. long
Lockwasher, No. 8
Front panel assembly (A10)
Front panel
Latch
Nasher, flat, No. 12
Fuse holder (XF1)
Fuse holder (XF2, XF3, XF9, XF10)
Fuse holder (XF5, XF7, XF9)
Fuse holder (spare)
use, 10 amp, slow blow (F5, F8 and spare)
Fuse, 3 amp, slow blow (F7, F9, F10 and spare)
(F1 and spare)
Screw, hexhead, No. 10-32, 5/8 in. long
Lockwasher, No. 10
lat, No. 10
Test point jack (TP2 thru TP5)
Test point jack (TP1)
hexhead, No 6-32, 3/8 in. long
. 6
Fuse cover
Screw, flathead, No. 6-32, 5/16 in. long
Side plate, lett hand

Screw, hexhead, No. 8-32, 3/8 in. long
Lockwasher, No. 8
asher, fiat, No. 8
位, left hand

Card guide
Screw, hexhead, No. 4-40, 1/ in. long
Lockwasher, No. 4
Washer, flat, No. 4

Polarizatir
Electrical receptacle connector (A9J4)
ce module component board assembly (A12)
Screw, hexhead, No. 10-32, 4-7/8 in. long
Screw, hexhead, No. 10-32, 6-3/8 in. long
kwasher, No. 10
Washer, fiat, No. 10
Capacitor nest
Capacitor, 82,000 of, 15 vdc (A9C2, A9C3)
Capacitor, 44,000 Of, 25 vdc (A9C4, A9C5)
Capacitor, 1500 of, 75 vdc (A9C1)
Screw, hexhead, No. 6-32, 5/8 in. long
Washer, flat, No. 6
Nus,
Screw, hexhead, No. 6-32, 3/8 in. long
Capacitor, 9200 of, 10 vdc (A9C7, A9C11)
Capacitor, $4600 \mu 20$ vdc (A9C8, A9C9)
Capacitor, $1200 \mu \mathrm{f}, 75 \mathrm{vdc}(\mathrm{A} 9 \mathrm{C} 10)$
capacitor bracket
Lockwasher, No. 6
Nasher, liat, No. 6
Endplate
Lockwasher, No. 6

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Washer, flat, No. 6
62.5 Side cover
62.6 Heatsink assembly (A4)
62.7 Screw, panhead, No. 6-32, 7/8 in. long
62.8 Lockwasher, No. 6
62.9 Washer, flat, No. 6
62.10 Heatsink assembly (A5)
62.11 Heatsink assembly (A6)

Screw, hexhead, No. 8-32, 3/8 in. long
Lockwasher, No. 8
Washer, flat, No. 8
Relay bracket
Screw, hexhead, No. 8-32, 3/8 in. long
Lockwasher, No. 8
Washer, flat, No. 8
Relay, 24 vdc (A9K1)
Grommet
Screw, hexhead, No. 6-32, 1/ in. long
Lockwasher, No. 6
Washer, flat, No. 6
Terminal board bracket
Stiffener
Screw, hexhead, No. 6-32, 5/8 in. long
Screw, hexhead, No. 6-32, 3/8 in. long
Hex nut, No. 6-32
Shield
Bracket
Standoff
Shield assembly
Lockwasher, No. 6
Washer, flat, No. 6
Terminal board (TB1)
Terminal board (TB2)
Component board assembly (A15)
Spacer
Screw, hexhead, No. 6-32, 5/16 in. long
Lockwasher, No. 6
Washer, flat, No. 6
Spacer
Nut, hex, No. 6-32
Screw, hexhead, No. 6-32, 3/8 in. long
Lockwasher, No. 6
Washer, flat, No. 6
Connector bracket assembly (A14)
Screw, hexhead, No. 4-40, 5/16 in. long
Lockwasher, No. 4
Washer, flat, No. 4
Component board assembly (AI)
Component board assembly (A2)
Component board assembly (A3)
Electrical receptacle connector (A9J1, A9J2, A9J3)
Polarization key
Nut, hex, No. 10-32
Lockwasher, No. 10
Washer, flat, No. 10
Nut, hex, 1/-20
Lockwasher, 1/4
Washer, flat, '/
Power transformer (A9T1)
Chassis
Clinch fastener, No. 6-32
Clinch fastener, No. 8-32
Clinch fastener, No. 10-32
Clinch fastener, No. 6-32
Eyelet
Chassis assembly
Drive motor on-off switch (TIG equipped units only)

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4-27. Removal and Replacement of Filter Assembly FLI
a. Removal. Remove filter assembly (21 fig. (4-5) as follows:
(1) Remove ac power from the punched tape reader.
(2) Remove the power supply PS2 as described in paragraph 4-25
(3) Remove the cables attaching to TB2 and E2. (Remove the cable clamp.)
(4) Remove the six nuts and pull out the filter assembly.
(5) Remove the external power cable from

TB1.
b. Replacement. To replace the filter assembly, reverse the removal procedure in a above.
4.28. Disassembly and Reassembly of Filter Assembly FLI
a. Disassembly. Disassemble filter assembly (21, fig. 4-5) by following the sequence of index numbers in figure 4-11.
b. Reassembly. To reassemble filter assembly, reverse the disassembly procedure in a above.

## 4-28.1 . Removal and Replacement of Relay and Filter Assembly

a. Removal. Remove relay bracket assembly (24.4, fig. 4-5) as follows:
(1) Remove ac power from the punched tape reader.
(2) Remove the power supply PS2 as described in paragraph 4-25
(3) Remove the wire.? attached to relay and filter assembly. (Be careful to note location for ease in replacing.)
(4) Remove the two screws, flat washers, and lockwashers (24.1, 24.2, and 24.2 , fig. 4-5) and pull out the relay assembly.
b. Replacement To replace the Relay and Filter Assembly, reverse the removal procedures in a above.

## 4-28.2 Disassembly and Reassembly of Relay and

 Filter Assemblya. Disassembly. Disassemble relay and filter assembly (24.4, fig. 4-5) by following the sequence of index number in figure 4-1-111
b. Reassembly. To reassemble relay and filter assembly, reverse the disassembly procedure in a above.

## 4-28.3 Removal and Replacement of Tape Clip Panel

a. Removal. Remove tape clip panel (6.1) fig. 4-5) by removing the eight screws (1, fig. 4-5), flat washers (2), and lockwashers (3), and separate the tape clip panel from the reader inclosure (27).
b. Replacement. To replace tape clip panel, reverse the removal procedure in a above.

## 4-28.4 . Disassembly and Reassembly of Tape Clip Panel

a. Disassembly. Disassemble tape clip panel by following the sequence of index numbers in figure 411.2.
b. Reassembly. To reassemble the tape clip panel, reverse the disassembly procedure in a above.


Figure 4-11.1. Relay and filter assembly, component location diagram.


[^2]4 Screw, panhead, No. 4-40, 1/2 in. long
5 Tape clip
6 Panel

Figure 4-11.2. Tape clip panel, component location diagram.


Figure 4-11. Filter assembly, component location diagram.

## Section V. DISASSEMBLY AND REASSEMBLY OF READER MECHANISM A2

## 4-29. General

Disassembly and reassembly of reader mechanism A2 is effected by removal and replacement of assemblies, subassemblies, and components as described in the following paragraphs. These paragraphs also describe the disassembly and reassembly of assemblies and subassemblies when not in the order of index numbers on exploded views. Use these procedures in conjunction with the trouble-shooting, repair, and adjustment procedures described ir paragraphs 4-9 through 415, and 4-45 through 4-62, respectively.
4-30. Removal and Replacement of Roller Support Assembly
a. Removal. Remove roller support (23, fig. 412) and the items mounted on it from panel (66) by loosening setscrews (24, 27, and 29) and screw (31).
b. Replacement. Insert roller support shaft (22) in panel (66) and assemble cam (28), tight tape spring (26), spring retainer (25), and stop (32) on the shaft. Position cam (28) so that when the roller support assembly is rotated counterclockwise in the tight tape condition, actuator (39) closes switch (40) when the tension on roller (16) is 105 to 120 grams. See para 461 for adjustment procedures.

## 4-31. Disassembly and Reassembly of Roller Support Assembly

a. Disassembly. Disassemble the roller support assembly in the order of the index numbers 15 through 23 in figure 4-12
b. Reassembly. Reassemble the roller support assembly in the reverse order of disassembly in a above.
$\rightarrow$ Secure by tightening screw (31) and setscrews (24, 27 and 28). 4-30

## 4-32. Removal and Replacement of Tape Deck Assembly

a. Removal. Remove tape deck assembly (47,fig. 4-12) from panel (66) as follows:
(1) Remove screw (8) and washers (8.1 and 9 ) and remove bottom cover (10).
(2) Remove carrier cover assembly (30, fig. 4-13.
(3) Remove screws (36), springs (37), and comb assembly (38).
(4) Remove two screws (46, fig. 4-12). Carefully lift tape deck assembly and disconnect wires from the connector.
b. Replacement. Replace the tape deck assembly in the reverse order of removal in a above.

4-33. Disassembly and Reassembly of Tape Deck Assembly
a. Disassembly. Disconnect leads and disassemble tape deck assembly (47 fig. 4-18) in the order of the index numbers in figure 4-13.
b. Reassembly. Reassemble tape deck assembly in the reverse order of disassembly in a above, except perform the tape motion sensor adjustment described in paragraph 4-60 before installing tape motion sensor (index numbers 14 through 19, fig. 4-13) in tape deck assembly (47, fig. 4-12). Before installing screw (22, fig. 4-13) and setscrew (28), prime the threads with Loctite primer, grade T. Secure screw (22), set screws (28) with Loctite sealant, Grade A.


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Figure 4-13. Tape deck assembly, exploded view.

| 1 | Screw, panhead, 4-40, $\mathrm{A} / \mathrm{in}$. long |
| :---: | :---: |
| 2 | Washer, plain, No. 4 |
| 2.1 | Lockwasher, internal tooth, No. 4 |
| 3 | Pivot pin |
| 4 | Actuator |
| 5 | Screw, panhead, 2-56, '/2 in. long |
| 6 | Lockwasher, internal tooth, No. 2 |
| 7 | Nut, hex, 2-56 |
| 8 | Washer, flat, No. 2 |
| 9 | Taper pin |
| 10 | Switch |
| 11 | Bracket |
| 11.1 | End of tape assembly |
| 12 | Screw, panhead, 4-40, 5116 in. long |
| 13 | Tape motion sensor holdown |
| 13.1 | Lockwasher, internal tooth, No. 4 |
| 13.2 | Shim, .003 in. thick |
| 13.3 | Shim, .0)5 in. Thick |
| 13.4 | Shim, .010 in. thick |
| 14 | Capstan shaft |
| 15 | Capstan |
| 16 | Taper pin |
| 17 | Not used |
| 18 | Not used |
| 19 | Housing |
| 19.1 | Tape motion sensor |
| 20 | Button assembly |
| 21 | Catch bolt spring |
| 22 | Screw, sockethead, 0-80, 3116 in . Long |
| 23 | Catch |
| 24 | Screw, panhead, 2-56, '/4 in. long |

*Includes set screws.

Washer, flat, No 2
Lockwasher, internal tooth, No 2
Tape motion sensor holddown
Dowel pin, 0125 dia $\times 7116$ in Ig
Holddown spring
Setscrew, socket, 4-40, 3/16 in long
Carrier shaft
Carrier cover assembly
Roller shaft
Not used
Roller
Screw, sockethead, 0-80, '. 4 in. long
Adjusting block
Shoulder screw
Comb spring
Comb
Carrier
Tape holddown assembly
Insert, latch
Screw, flat head, 1-72, 3116 in . Ig
Grip ring
Dip spring waslier
Not used
Tape guide assembly*
Screw, panhead, 2-56, 1/4 in. long
Lockwasher, internal tooth, No 2
Washer, plain, No 2
Bracket assembly
47 Tape deck
Not used
Bracket shim, 010 in. thick

## Fiqure 4-13-Continued

## 4-34. Removal and Replacement of Read Head and Track Assembly

a. Removal. Remove read head and track assembly (54 fig. 4-12) as follows:
(1) Remove tape deck assembly (47) as described in paragraph 4-32れ.
(1.1) Disconnect taper pins from terminal block using pin removal tool No. 380305-1 (NSN 5120-00-772-2467).
(2) Remove two screws (52) and lockwashers (53) and carefully lift read head and track assembly (54) off capstan (51) and away from capstan drive mechanism assembly (64).
(3) Clean the assembly in a bath of Freon TF. Allow the solution to dry, then use a vacuum cleaner to remove any remaining dust particles.

## CAUTION

Take care not bend the spring contacts while cleaning.
b. Replacement. Perform adjustment procedures described in paragraphs 4-48 4-49, and 4-50 before replacing the read head and track assembly. Replace as follows:
(1) Carefully place read head and track assembly (54) over capstan (51) and against capstan drive mechanism assembly (64), and secure by installing two screws (52) and lockwashers (53).
(2) Perform the capstan height
outlined in paragraph 4-13
(3) Replace wiring by inserting taper pins in terminal blocks fig. 8-6).
(4) Perform the contact pressure adjustment as outlined in paragraph 4-5.
(5) Replace the tape deck assembly as described in paragraph 4-32hb.
(6) Perform the timing adjustment procedures as outlined in paragraph 4-52

## 4-35. Disassembly and Reassembly of Read Head and Track Assembly

a. Disassembly. Disassemble read head and track assembly (54. fig. 4-18) in the order of the index numbers in figure 4-14
b. Reassembly. Reassemble read head and track assembly in the reverse order of disassembly in a above. Before installing screws (2, 4, fig. 4-14) prime the threads with primer, sealing compound, NSN 8030-00-145-0001 (Locktite, grade T). Secure screws (2 and 4) with sealing compound, retaining, NSN 8030-00-0812339 (Locktite, grade A).

## CAUTION

When soldering wires to plastic contacts, use an adequate heat sink to prevent heat damage to the plastic contacts.
Perform the adjustments described in paragraphs 4-48. 4-49 and 4-50.


Figure 4-14. Read head and track assembly, exploded view.

## 4-36. Removal and Replacement of Amplifier

 Assemblya. Removal. Remove amplifier assembly (61, fig 4-12) by disconnecting the leads and removing four screws (60).
b. Replacement. Replace the amplifier assembly by placing it against chassis gusset (110), installing four screws (60), and connecting the leads as shown in figure 8-6.

4-37. Disassembly and Reassembly of Amplifier Assembly
a. Disassembly. Disconnect leads and disassemble amplifier assembly (61, fig. 4-1) in the order of the index numbers in figure 4-15
b. Reassembly. Reassemble the amplifier assembly in the reverse order of disassembly in a above.


Figure 4-15. Amplifier assembly, A2, part location diagram.

## 4-38. Removal and Replacement of Capstan Drive

 Mechanism Assemblya. Removal. Remove capstan drive mechanism assembly (64 fig. 4-12) as follows.
(1) Remove screw (3) and lockwasher (4) and lift capstan drive guard (5) off capstan drive mechanism assembly (64).
(2) Remove two screws (6) and lift off fan guard (7).
(3) Slide drive belt (48). off 14-tooth pulley (50).
(4) Loosen setscrew (49) and slide 14tooth pulley (50) off shaft and gear assembly (38, fig. 416).
(5) Remove tape deck assembly (47 fig. 4-12) as described in paragraph 4-32a.
(6) Remove read head and track assembly (54) as described in paragraph 4-34a.
(7) Slide capstan (51) off capstan shaft (31, fig. 4-16).
(8) Disconnect the leads.
(8.1) Loosen setscrew (56 fig. 4-12), remove slew lever (58), and push out slew cam (55). Pull out push rod (94) far enough to clear capstan drive assembly (64).
(9) Remove four screws (62, fig. 4-12 and lockwashers (63) and carefully lift capstan drive mechanism assembly (64) back out of panel (66).
b. Replacement. Replace capstan drive mechanism assembly as follows:
(1) Carefully place capstan drive mechanism assembly (64) in position against panel (66) and secure by installing screws (62) and lockwashers (63).
(2) Connect leads.
(3) Slide capstan (51) on capstan shaft (31, fig. 4-16).
(4) Replace read head and track assembly (54, fig. 4-12) as described in paragraph 4-34b.
(5) Replace tape deck assembly (47) as described in paragraph 4-32h.
(6) Slide 14-tooth pulley (50) on shaft and gear assembly (38. fig. 4-16), align with pulley on drive motor (68,fig. 4-12), and secure by tightening setscrew (49).
(7) Slide drive belt (48) on 14-tooth pulley (50).
(8) Place fan guard (7) in position and secure by installing two screws (6).
(9) Place capstan drive guard (5) in position and secure by installing screw (3) and lockwasher (4).
(10) Replace push rod (94), slew cam (55), slew lever (58), and tighten setscrew (56). Then perform the slew lever adjustment procedure as outlined in paragraph 4-60.1.
(11) Perform timing adjustment as described in paragraph 4-52

## 4-39. Disassembly and Reassembly of Capstan Drive Mechanism Assembly

a. Disassembly. Disassemble capstan drive mechanism assembly (64, fig. 4-12) in the order of the index numbers in figure 4-16.
b. Reassembly. Reassemble capstan drive mechanism assembly in the reverse order of disassembly in a above, except as follows:
(1) When assembling wheel and gear assembly (17, fig. 4-16), differential spider bevel gear (22), differential spider assembly (23), capstan shaft (31), shaft and gear assembly (38), and associated parts, install the proper thickness of shims (18, 21, and 37) necessary to meet the end play requirements specified ir paragraphs 4-53 through 4-56.
(2) After assembling the magnetic actuator assembly (index numbers 41 through 51), but before attaching the assembly to adjusting plate assembly (56), perform the adjustment procedures described in paragraphs 4-57 and 4-58
(3) When attaching bracket (50, fig. 4-16 to frame (51), assure that the shoulder of bracket (50) is flush with the top edge of frame assembly (51) to within .001 inch. After attaching the magnetic actuator assembly to the adjusting plate assembly (56, fig. 4-16 with screws (39), attach adjusting plate assembly to frame (61). Torque the adjusting plate lock screw (53) to 17 to 21 inch pounds, Perform the adjustment procedure described in paragraph 4-59. Apply glyptol to screw head (52, fig. 4-16 and to setscrew (52).
(4) Before replacing bushings (57 through 60, fig. 4-16), prime them with Loctite, Grade T sealing compound. Insure a press fit by applying Loctite, Grade A sealing compound between each bushing and frame (61).

Change 6 4-37


Figure 4-16. Capstan drive mechanism assembly, exploded view.

| 1 | Screw, flathead, No. 8-32, 1/2 in. long |
| :---: | :---: |
| 2 | Adapter plate |
| 3 | Screw, pinhead, No. 4-40, 1/4 in. long |
| 4 | Lockwasher, internal tooth, No. 4 |
| 5 | Terminal strip |
| 6 | Screw, panhead, No. 4-40, 1/4 in. long |
| 7 | Lockwasher, internal tooth, No. 4 |
| 7.1 | Washer, flat, No. 4 |
| 8 | Tape slewing spring |
| 9 | Pivot pin |
| 10 | Latch assembly |
| 11 | Screw, sockethead, No. 4-40, 1 in . long |
| 12 | Lockwasher, internal tooth, No. 4 |
| 12.1 | Washer, flat, No. 4 |
| 13 | Latch pivot block |
| 14 | Screw, sockethead, No. 8-32, 1/2 in. long |
| 15 | Lockwasher, internal tooth, No. 8 |
| 15.1 | Washer, flat, No. 8 |
| 16 | Rod mounting block |
| 17 | Wheel and gear assembly |
| 18 | Shim, .003 in. thick |


| 18.1 | Shim, .005 in. thick |
| :--- | :--- |
| 18.2 | Shim, . 010 in. thick |
| 19 | Roll p;h |
| 20 | Retaining ring |
| 21 | Shim, .003 in. thick |
| 21.1 | Shim, .005 in. thick |
| 21.2 | Shim, . 010 in. thick |
| 22 | Differential spider drive gear |
| 23 | Differential spider capstan |
| 23.1 | Spider gear assembly |
| 24 | Wave washer |
| 25 | Screw cap' |
| 26 | Spring washer' |
| 27 | Friction washer' |
| 28 | Clutch drive gear' |
| 29 | Friction washer, |
| 30 | Hub friction clutch assembly' |
| 31 | Capstan shaft |
| 32 | Setscrew, socket, No. $4-40$, |
| 3 | 3/16 in. long |
| 33 | Cluster gear assembly |
| 34 | Cluster gear assembly |
| 35 | Thrust washer |
| 36 | Idler shaft |
| 37 | Shim, .003 in. thick |
| 37.1 | Shim, . 005 in. thick |
| 37.2 | Shim, . 010 in. thick |
| 38 | Shaft and gear assembly |
| 39 | Screw, sockethead, No. $4-40$, |
|  | $1 / 8$ in. long | 1/8 in. long

Figure 4-16-Continued.

40 Not used
41 Stop nut, No. 6-32
42 Spring tension adjust screw
43 Actuator spring
44 Armature assembly
45 Antiresidual shim
46 Screw, panhead, No. 4-48, 1/8
in. long
47 Washer, split ring, No. 4
48 Escapement limit
49 Screw, panhead, No. 4-48, 1/8 in. long
50 Actuator bracket
51 Coil and frame assembly
51.1 Actuator assembly

52 Setscrew, sockethead, No. 6$32,1 / 2$ in. long
53 Screw, sockethead, No. 6-32, 1/2 in. long
54 Lockwasher, internal tooth, No. 6
55 Washer, flat, No. 6
56 Adjusting plate assembly
57 Bushing
58 Bushing
59 Bushing
60 Bushing
61 Frame

## 4-40. Removal and Replacement of Motor

a. Removal. Remove motor (75 fig. 4-12) as follows:
(1) Remove screw (3) and lockwasher (4), and lift capstan drive guard (5) off capstan drive mechanism assembly (64).
(2) Remove screw (6) and lift off fan guard (7).
(3) Slide drive belt (48) off 10-tooth pulley (68).
(4) Loosen setscrew (67) and slide 10tooth pulley (68) off the motor shaft.

NOTE
Motor pulley is 12 tooth for 50 cps power and 10 tooth for 60 cps power.
(5) Loosen setscrew (69) and slide fan (70) off the motor shaft.
(6) Disconnect terminals (71).
(7) Remove two screws (72), lockwashers (73), and flat washers (74) and carefully lift motor (75) off base chassis assembly (111).
b. Replacement. Replace the motor as follows.
(1) Carefully place motor (75) in position
chassis assembly (111) and loosely secure by installing two screws (72), lockwashers (73), and flat washers (74).
(2) Connect terminals (71).
(3) Slide fan (70) on the motor shaft and secure by tightening setscrew (69).
(4) Slide 10-tooth pulley (68) on the motor shaft and secure by tightening setscrew (67).
(5) Slide drive belt (48) on 10-tooth pulley (68). Adjust belt tension and tighten motor mounting screws as described in paragraph 4-53.1.
(6) Place the fan guard (7) into position and secure it in place with two screws (6).
(7) Place capstan drive guard (5) in position and secure by installing screw (3) and lockwasher (4).

## 4-41. Disassembly and Reassembly of Motor

a. Disassembly. Disassemble motor (75, fig. 4 12) in the order of the index numbers infigure 4-17
b. Reassembly. Reassemble the motor in the reverse order of disassembly in a above.

Change 8 4-38.2


Figure 4-17. Motor, exploded view.
Change 4 4-38.3

## 4-42. Removal and Replacement of Wiring Harness Assembly

a. Removal. Remove network assembly (89, fig. 4-12), bracket (92), and the items mounted on them from base chassis assembly (111) by removing two screws (76), two plain washers (77), two plastic clamps (78), three screws (79), three lockwashers (80), lockwasher (81), two screws (82), two screws (83), two nuts (84), two lockwashers (85), and two plain washers (86). Disconnect all leads and lift wiring harness assembly (index numbers 87 through 93) off base chassis assembly (111).
b. Replacement. Replace wiring harness assembly (index numbers 87 through 93, fig. 4-12) by placing it in position on base chassis assembly (111), connecting all leads as shown ih figure 8-6, and installing all attaching hardware removed in a above.

## 4-43. Disassembly and Reassembly of Wiring Harness Assembly

a. Disassembly.

Disassemble the wiring harmless assembly in order of the index numbers 87 through 93 in figure 4-12. Disassemble the network assembly (89) in the order of the index numbers in figure 4-18.
b. Reassembly. Reassemble wiring harness assembly (index numbers 87 through 93, fig. 4-12) in the reverse order of disassembly in a above.


Figure 4-18. Network assembly A1, exploded view.

## Section VI. REPAIRS AND ADJUSTMENTS

## 4-44. General

The following paragraphs describe the mechanical repairs and electrical and mechanical adjustments required to maintain the punched tape reader. All adjustments to reader mechanism A2 must be made when the unit is cold. If the unit has been operating, wait at least ten minutes before making any adjustment, since temperatures rise enough during operation to expand tolerances.

## 4-45. Repair

Repair normally consists of removing and replacing a defective part as described in the removal and replacement or disassembly and reassembly procedures given in sections IV and V.

## 4-46. Spring Data

Use the following data to determine whether a spring meets the tension or compression requirement and also as a menas of identifying springs.
Replace all springs that do not meet the torsion, compression, or tension requirements.
a. Tight Tape Spring. The tight tape spring (26, fig. 4-12) is shown in A, figure 4-19. The torque required to deflect the spring to its final position is 105 gram-in.
b. Catch Bolt Spring. The catch bolt spring (21, fig. 4-13) is shown in B, figure 4-19. The force required to compress the spring to its compressed length is 14 to 18 oz .
c. Holddown Spring. The holddown spring (27, fig. 4-13) is shown in C, figure 4-19. The torque required to deflect the spring to its final position is 118 to 138 gram-in

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d. Comb Spring. The comb spring (37, fig 413) is shown in D, figure 4-19
e. Actuator Spring. The actuator spring (43, fig. 4-16 is shown in $E$, figure 4-19. The force required to provide initial tension on the spring is 120 to 170 grams.

## 4-47. Adjustments

The following paragraphs describe adjustment and alignment procedures and tolerance requirements for the punched tape reader. Adjustment procedures are arranged in the proper sequence for a complete readjustment of the punched tape reader. When making individual adjustments, check all related adjustments. Where removal of parts or subassemblies is necessary to make an adjustment, reference is made to specific

paragraphs for removal and replacement instructions.
(Also, see bara. 4-1\% thru 4-14.)

## NOTE

Before proceeding with the read head adjustment, check the roller ( 33 , fig. 4-13), to determine if it is worn and replace if necessary.

4-48. Read Head Fixed Contact Adjustment Remove the tape deck assembly as described in paragraph 4-32 and adjust read head and track assembly as follows:
a. Requirement. Each of the eight fixed contact assemblies must extend above the fixed contact support between 0.290 and 0.300 inch.

Figure 4-19. Spring data
b. Adjustment. Adjust the appropriate height adjustment screws on the fixed contact support to achieve the required fixed contact height.

Note. It may become necessary to readjust individual fixed contact assemblies for proper contact switching. Do not readjust all fixed contact assemblies to the required height unless complete read head readjustment or replacement is required. Refer to paragraph 4-52d(2) for additional requirements for individual fixed contact adjustments.
4-49. Read Head Movable Contact Adjustment ffig. 4-21).
Remove the tape deck assembly as described in paragraph L-32 and adjust the read head movable contact as follows:
a. Requirement. The movable wire contacts must be free to move up and down in the gap of the fixed contact.
b. Adjustment. Correct improper alignment by laterally adjusting the fixed contact support. To adjust, loosen the support mounting screws and
carefully move the fixed contact support until all wire contacts are centered in the fixed contact gaps. Retighten the mounting screws.



Figure 4-20. Read head fixed contact requirement.

## 4-50. Starwheel Height Adjustment

(fig. 4-22)
Remove the tape deck assembly as described in paragraph 4-32d and adjust the starwheel height as follows:
a. Requirement. With starwheel height gage 361500 mounted in mounting holes ordinarily used for installation of the tape deck assembly, the starwheels must raise the gage pins to 0.000 to $\pm 0.002$ inch from top of gage.

Note. When using gauge with stepped top surface,
measurements must be made from the high surface (left side as viewed in fig. 4-22).
b. Adjustment. Correct starwheel height by loosening the locking screws on the movable contact bracket. Adjust bracket height by varying the setscrews on the top of the bracket. Retighten the locking screws.

Note It may not be possible to adjust the starwheels as low a specified. In this case, adjust the bracket height as low as possible. All pins should be uniform in height to insure proper positioning of the movable contacts.


Figure 4-22. Starwheel height requirement.

## 4-51. Contact Pressure Adjustment

Remove the tape deck assembly as described in paragraph 432, remove the bottom cover, and adjust read head and track assembly as follows:
a. Requirement. The contact pressure required to lower the movable wire contacts, when switch contact is broken, must be at least 6 grams for each contact.
b. Method of Checking. Check each contact pressure with the starwheel in the "hole" position (fig. 3$6)$.
c. Adjustment. With gram gage 4043403, (3 to 30 grams, FSN 5210-799-2106) and a wire tool, apply a force to the movable wire contact (but not against it) [fig. 4-23). Increase contact pressure by lowering the fixed contact assembly with the height adjustment screw, and raising the movable wire contact with the setscrew.

## NOTE

1. Use a paper clip to make a wire tool similar to that shown in fig. 4-23. Form a $1 / 4$-inch loop at the upper end of the tool.
2. The point at which contact is broken can be determined easily by observing the deflection on an ohmmeter connected as follows: Remove power from the equipment. On the backplane, connect one ohmmeter lead to XA3, pin A. connect the other lead to pin 1 on TB1 of the read head (A2TB1 or A4ITB1), and observe the switching of movable contact No. 1. Repeat procedure with pins 2 through 8 , and movable contacts 2 through 8.

Change 7 4-38.7


Figure 4-23. Contact pressure requirement.

## 4-52. Timing Adjustment

Remove the capstan drive guard as described in paragraph 4-38 and adjust the capstan drive mechanism as follows:
a. Requirement. Contact switching must occur within the limits of $2.5 \mathrm{~ms}(\mathrm{~min})$ and 6.2 ms (max) with respect to the leading edge of the tape drive pulse as shown by figure 4-23.1.

Note. The ideal waveform is a square
wave with all transitions occuring approximately 4.3 ms after the leading edge of the tape drive pulse with no extra pulses (indicating contact bounce). Adjustments should be performed to bring the waveform as close to the ideal as possible.
b. Method of Checking. Using a dual-trace preamplifier with oscilloscope, connect the Channel A probe to J4-L of the logic assembly to obtain the tape drive pulse. Run the alternate hole test pattern tape (alternate "U" and "*" characters) through the reader. In sequence, connect the oscilloscope Channel B probe to pins $3, \mathrm{E}, \mathrm{H}, \mathrm{K}, \mathrm{M}, \mathrm{P}, \mathrm{S}$ and U of A1J3 (fig. 8-1), step the tape and note whether or not the contact switching time of each data pulse meets the requirement(fig. 4-23.1).

Note. The positive and negative going transitions must both be observed and measured, since one of them may be well within tolerance and the other may be out. This may require starting and stopping the tape
reader until both transitions have been observed on the oscilloscope.
c. Adjustment. The adjustments described in baragraphs 4-48 through 4-51 should precede this adjustment.
(1) Loosen the clamp screw (fig. 4-25) and turn the adjusting screw counterclockwise to advance the tape, or clockwise to delay the tape. If this adjustment does not provide correct timing, insert a short length of alternate hole pattern tape in the punched tape reader. Remove the roll pin on the differential spider. With the motor running, turn the capstan shaft manually until starwheels sensing no-holes are equally spaced between holes (fig. 4-24), Install the roll pin and readjust as previously specified. Upon completion of adjustment, torque the clamp screw to 17-21 inch-pounds and apply glyptol to the heads of the clamp and adjusting screws.
(2) If the checks in $b$ above show that one or more (but no all) contacts switch outside the allowable region, adjustment of the individual fixed contact(s) is required. While observing the switching time of the contact with the oscilloscope as described in the method of checking above, turn the height adjustment screw [fig. 4-23) to raise or lower the fixed contact until it meets the timing requirement.


Figure 4-23.1. Contact switching timing.

## 4-38.8.1 Change 7



Figure 4-24. Starwheel positioning.
Change 8 4-38.8.2


Figure 4-25. Timing requirement.

4-53. Motor Input Shaft Endplay Adjustment (fig. 4-26)
a. Requirement. Motor input shaft endplay must be between 0.005 and 0.015 inch.

NOTE
If requirement is not met, remove and disassemble the capstan drive mechanism assembly as described in paragraphs 4-38 and 4-39, and adjust for motor shaft input endplay. Also, before disassembly, check to insure that other endplay adjustments in paragraphs 4--51 through 4-56 are within tolerances.
b. Adjustment. When reassembling the motor input shaft, gears, bearings, washers, and other components, insert the proper thickness of shims between the shaft and gear assembly and the bushing to provide the required endplay.

## 4-53.1. Timing Belt Tension Adjustment

a. Requirement. Belt deflection at the midpoint of its span should be $3 / 16+1 / 16$ inch with a force of 150 grams applied.
b. Adjustment. Loosen two screws (72, fig. 4-12), move the motor (75) to obtain proper belt tension, and tighten the screws (72).


Figure 4-26. Endplay requirements.

4-54. Idler/Drive Bevel Gear Endplay Adjustment (fig. 4-26)
a. Requirement. Idler/drive bevel gear adjustment endplay must be between 0.001 and 0.010 inch.

## NOTE

If requirement is not met, remove and disassemble the capstan drive mechanism assembly as described in paragraphs 4-38 and 4-39, and adjust for idler/drive bevel gear endplay. Also, before disassembly, check to ensure that other endplay adjustments in paragraphs 4-53 through 4-56 are within tolerances.
b. Adjustment. When reassembling idler/drive bevel gear, shafts, bearings, washers, and other components, insert the proper thickness of shims between the idler/drive bevel gear and the bushing to provide the required endplay.

## 4-55. Capstan Shaft Endplay Adjustment

 (fig. 4-26)a. Requirement. Capstan shaft endplay must be between 0.002 and 0.006 inch.

## NOTE

If requirement is not met, remove and disassemble the capstan drive mechanism assembly as described in paragraphs 4-38 and 4-39, and adjust for capstan shaft endplay. Also, before disassembly, check to insure that other endplay adjustments in paragraphs 4-53 through 4-56 are within tolerances.
b. Adjustment. When reassembling the capstan shaft, gears, bearings, washers, and other components, insert the proper thickness of shims between the wheel and gear assembly and the bushing to provide the required endplay.

## 4-56. Spider Bevel Gear Endplay Adjustment

 (fig. 4-26)a. Requirement. Spider bevel gear endplay must be between 0.001 and 0.006 inch.

## NOTE

If requirement is not met, remove and disassemble the capstan drive mechanism assembly as described in paragraphs 4-38 and 4-39, and adjust for spider bevel gear endplay. Also, before disassembly, check to ensure that other endplay adjustments in paragraphs 4-53 through 4-56 are within tolerances.
b. Adjustment. When reassembling the spider bevel gear, shafts, bearings, washers, and other components, insert the proper thickness of shims between the spider bevel gear and the E ring to provide the required endplay.

## 4-57. Return Spring Force Adjustment

 (fig. 4-27)a. Requirement. Armature return spring tension must be $225( \pm+50)$ grams.
b. Method of Checking. Hook gram gage 4043402 at the point indicated in figure 4-27 and lift the armature tip gently to measure spring tension.

## NOTE

If requirement is not met, remove the capstan drive mechanism assembly as described in paragraph 4-38 and adjust for requirement in a above.
c. Adjustment. Adjust the setscrew which is attached to the armature return spring to meet the requirement.

## 4-58. Heel Gap Adjustment

## (fig. 4-28)

a. Requirement. The gap between the heel of the armature and the upper edge of the slot in the armature limit must be between 0.016 and 0.018 inch.


Figure 4-27. Return spring force requirement.
b. Method of Checking. Insert a 0.016 -inch feeler gage into the slot of the armature limit as shown in figure $4-28$. The gage must slip in easily. Insert a 0.018 -inch feeler gage into the slot of the armature limit. This gage must slip in with perceptible drag.

## NOTE

If requirement is not met, remove and disassemble the capstan drive mechanism assembly as described in paragraphs 4-38 and 4-39, and adjust for requirement in a above. Also, before disassembly, check to ensure that endplay adjustments in paragraphs 4-53 and 4-56 are within tolerances.
c. Adjustment. Loosen the screw and insert the 0.018 -inch feeler gage. Press the armature limit firmly against the gage until the requirement is met, and tighten the screw. Be careful that the coil frame does not pivot on the bracket.

## 4-59. Tip Clearance Adjustment

(fig. 4-29)
a. Requirement. The clearance between the armature tip and the escapement tooth must be between 0.008 and 0.010 inch.
b. Method of Checking. Insert the 0.018 -inch feeler gage into the slot of the armature limit. Turn the clutch so that the flat of an escapement tooth rests under the armature tip. Insert a 0.008 -inch feeler gage between the armature tip and the escapement tooth. The gage must slip in easily. Insert a 0.010 -inch feeler gage between the armature tip and the escapement tooth. This gage must slip in with perceptible drag.

## NOTE

If requirement is not met, remove and disassemble the capstan drive mechanism assembly as described in paragraphs 4-38 and 4-39, and adjust for requirement in a above. Also, before disassembly, check to ensure that endplay adjustments in paragraphs 4-53 through 4-56 are within tolerance.


Figure 4-28. Heel gap requirement.
c. Adjustment. Loosen the mounting screws. Place a small screwdriver or awl between the mounting screws and the bracket, and rotate the assembly in the direction necessary to meet the requirement. Retighten the mounting screws.

An alternate method of adjustment is to tap the assembly as necessary; at the bottom to reduce clearance, and at the top to increase clearance. Be careful to avoid distorting the coil frame or bracket as shown in figure 310.

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Engage the end of the gram gage into a sprocket hole in the leading end of the tape. Hold the trailing end of the tape firmly, slowly move the gram gage to the left to pull the leading end of the tape in the direction of normal tape travel, and note the tension required to start the top of the roller support moving to the left.
c. Adjustment. Loosen the setscrew and rotate the spring retainer to preload the spring until the requirement is met (fig. 4-31).


Figure 4-31. Tight tape sensor positioning requirement.

## 4-62. Roller Support Shaft Endplay Adjustment

(fig. 4-32)
a. Requirement. Roller support shaft endplay must be 0.01 to 0.02 inch between the grip ring and the end of the roller assembly.
b. Adjustment. When installing the grip ring on the roller support shaft, provide the required endplay.


Figure 4-32. Roller support shaft endplay requirement.

## 4-63. Adjustment of Power Supply Output Voltages

a. Requirement. The adjustment of the power supply output voltages is an electrical adjustment which is made by means of four potentiometers to produce the specified dc output voltages at specific test points within the power supply. These adjustments are made with the power supply connected into the punched tape reader and the power on.
b. Method of Checking. Connect a digital voltmeter to the following test points at the front panel of the power supply. The dc voltages measured should fall within the tolerances specified.

| Test point | Voltage tolerance (dc) |
| :---: | :---: |
| +4.75 and COM | +4.75 t0.06 |
| --12V and COM | $-12,00+0.06$ |
| +12 V and COM. | $+12.00+0.06$ |
| --48V and COM ........ | $-48.00+0.24$ |

c. Adjustment. If any of the voltages specified in b above are out of tolerance, the corresponding potentiometer should be adjusted to bring the voltage within tolerance. The potentiometers are listed as follows:

|  |  | Fig. 4-10 |
| :---: | :---: | :---: |
| Dc voltage | Potentiometer to be adjusted | item No. |
| +4.75 | R24 on card A1 | 92 |
| +12 | R17 on card A2 ................... | 93 |
| -12 | R32 on card A2 | 93 |
| -48 | R18 on card A3 | 94 |

## 4-64. Adjustment of Power Supply Regulated Supply

a. Requirement. After the power supply output voltage adjustments are performed, the performance of the regulated supply located on card A12 in the power supply should be checked.

CAUTION
When taking voltage measurements on power supply PS1 sequence module A12, use insulated test connectors to avoid possible short circuits between test points and copper runs.
b. Method of Checking. Connect a digital voltmeter between the test points TP11 (+) and TP13 (common) located on card A12 in the power supply (40, fig. 4-10. The test points are clearly labelled on the card. The power supply should be operating in the normal manner in the tape reader, with normal system power turned on. The voltage measured should be $+15.0 \pm 0.1 \mathrm{vdc}$.
c. Adjustment. If the voltage from test point TP11 to TP13 is not within tolerance, adjust potentiometer R73 on card A12 (40, fiq. 4-10).

## 4-65. Adjustment of Power Supply Over-voltage Limit

a. Requirement. After the +4.75 -output voltage has been checked and adjusted (para 4-3), the overvoltage limit circuit for the +4.75 -volt output should be checked to make certain that the trip point of 5.5 vdc is not exceeded.
b. Method of Checking.
(1) Disconnect wire connection from PS1TB2, pin 2.
(2) Connect a digital voltmeter to the test point labeled $4.75(+)$ on the power supply front panel and the COM test point.
(3) Slowly adjust potentiometer PS1A1R24 to obtain an increase in the +4.75 volt output, while observing the digital voltmeter. Continue to increase the voltage, while observing the voltmeter, until the meter indication suddenly drops to zero volts. The maximum voltmeter indication (which occurs immediately before the voltage drops to zero), is termed the "trip point" and should be 5.40 volts dc $(-0.05)$.
c. Adjustment.
(1) If the trip point voltage is out of tolerance, adjust potentiometer PS1AIR30. Repeat the check and adjustment until the trip point voltage is within the specified tolerance.
(2) Adjust PS1A1R24 to meet the requirements of paragraph 4-3
(3) Disconnect the digital voltmeter.
(4) Reconnect the wire connection to PS1TB2, pin 2.

## 4-66. Oscillator Frequency Adjustment (PC Card A1)

Adjust the oscillator frequency during initial installation of the tape reader and whenever a new PC card AI is installed. Connect a frequency counter (Beckman model 7350A or equal) to pin T of PC card connector XA1; connect the other lead to ground.

With power on, adjust potentiometer R20 fig. 5-7 to obtain a frequency indication of 9.6 KHZ ( $\pm 1$ percent).

Note. If a frequency counter is not available, adjust R20 for 104 microseconds using an oscilloscope.

## 4-67. General

a. Scope. This section contains the parts list, step-by-step installation procedures, and checkout procedures required to convert a single punched tape reader into a dual punched tape reader.
b. Power. It is imperative that power to the punched tape reader be turned off and disconnected during installation of this conversion kit. Thus, the tape send channel must be off-line during conversion.
c. Manpower required. To prevent damage to equipment and injury to personnel, two men are required to perform the conversion.

Table 4-1. Parts List for Dual Punched Tape Reader Conversion Kit

| $\begin{gathered} \hline \text { Item } \\ \text { No } \\ \hline \end{gathered}$ | Qty | Part number | Name |
| :---: | :---: | :---: | :---: |
| 1 | 1 | *A64780-001. Tally Corp. Seattle, Washington, Part No. 347910 composed of Tally Corp. Envelope Part No. 347930 and Tally Corp. 12 Tooth Motor Pulley Part No. 2204433. | Ancillary Item; conversion kit, composed of 12 tooth motor pulley and envelope. |
| 2 | 24 | *A64779-001----------------------------------------------1-1-- | Ancillary item; clip tape. |
| 3 | 1 | *A53930-001. Tally Corp., Seattle, Washington, Part No. 305089. | Running spare, timing belt. |
| 4 | 8 | AN960C10L------------------------------------------------------ | Washer, flat. |
| 5 | 8 | MS35338-138 ------ | Washer, lock. |
| 3 | 1 | *A64757-001- | Reader mechanism assembly. |
| 7 | 10 | *SM-B-583244-008 ----------------------------------------- | Sealing compound. |
| 8 | 2 | *A61666-001- | Cable assembly, special purpose, electrical. |
| 9 | 1 | *A64758-002- | Control panel assembly. |
| 10 | 7 | *SM-C-546211-9-- | Clamp, cable. |
| 11 | 1 | *SM-C-546211-8----------------------------------------- | Clamp, cable. |
| 12 | 9 | MS5157-46 -------------------------------------------------------- | Screw, machine, pan head. |
| 13 | 11 |  | Washer, lock. |
| 14 | 15 | AN960C8L | Washer, flat. |
| 15 | 12 | MS35649-284 -------------------------------------------------- | Nut, plain, hex. |
| 16 | 1 | *SM-C-546211-12--------------------------------------------- | Clamp, cable. |
| 17 | 55 | MS17821-1-9-------------------------------------------------- | Tie wrap. |
| 18 | 1 | *A64752-001-- | Logic assembly. |
| 19 | 1 | *SM-C-634816 | Bar, cable. |
| 20 | 1 | *A64776-001- | Relay and filter assembly. |
| 21 | 2 | MS51958-63- | Screw, pan head. |
| 22 | 1 | MS51957-30-- | Screw, machine pan head. |
| 23 | 3 | *SM-C-546211-11 | Clamp, cable. |
| 24 | 1 | AN960C6L | Washer, flat. |
| 25 | 9 | MS35338-136 | Washer, lock. |
| 26 | 1 | MS35649-264 | Nut, plain, hex. |
| 27 | 8 | AN960C6 | Washer, flat. |
| 28 | 8 | *SM-B-546131 | Locking screw. |
| 29 | 1 | *SM-D-546279 | Slide. |
| 30 | 4 | 639123-468 | Screw, machine. |
| 31 | 1 | *810003-103---------------------------------------------- | Power supply. |
| 32 | 4 | MS35335-59 | Washer, lock. |
| 33 | 1 | *SM-C-634831-1-- | Clamp, cable support. |
| 34 | 1 | *A64775-001- | Plate, reference. |
| 35 | 1 |  | Change 3 to Technical Manual Reader, Punched Tape RP-154 (P)/G. |
| 36 | 2 | *555557-022------------------------------------------- | Strip, fanning. |
| 37 | 2 | *V00078-004---- | Adapter, Bulkhead. |

*General Dynamics Part Number.

## 4-69. Installation Procedure

a. Preliminary procedure.
(1) Check the conversion kit parts against the parts list table 4-1) to verify that all of the necessary parts are contained in the kit.
(2) Store ancillary items and running spares (items 1, 2, and 3 table 4-7) with other station ancillary items and running spares.
(3) For safety, turn off the 120 volts ac power to the punched tape reader; then disconnect the input power cable from TB-1 (16, fig. 4-1]) of the filter assembly (21 fig. 4-5).
(4) Remove the top rear panel from the punched tape reader enclosure. Reinsert the panel mounting screws (with washers attached) in the panel mounting holes (to prevent loss of mounting hardware).
(5) Remove the tape clip panel (6,fiq. 4-11,2) from the reference designation AS area (fig. 1-3). Remove washers from mounting screws and store them with their corresponding parts of the conversion kit (items 4 and 5, table 4-1). Store the hex nuts for later use. The screws will no longer be required.
(6) Remove all tie wraps binding unterminated cables to enclosure structure.
b. Reader mechanism installation.
(1) Remove the outer chassis slides and mounting hardware (part of 9, fiq. 4-7) from the reader mechanism (item 6, table 4-1).


1. APPLY SEALING COMPOUND SM-B-583244-008 TO SCREW THREADS BEFORE AND AFTER FINAL TIGHTENING.
2. ALL HARDWARE SHOWN IS SUPPLIED AS PART OF SLIDE.
3. RIGHT HAND SLIDE SHOWN. INSTALL LEFT HAND SIIDE IN SIMILAR MANNER.

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Figure 4-33. Reader mechanism assembly slide installation details, exploded view.
(2) Install the outer slides inside the enclosure as shown in figure 4-33 (holes are provided for mounting slides in reference designation A5 area of enclosure). Do not apply sealing compound to the screw threads at this time because it may be necessary to slightly reposition the slides for proper operation when the reader mechanism is installed.
(3) Install the reader mechanism (para 4-19).
(4) With the reader mechanism installed, reposition the outer slides, if necessary; then apply sealing compound (item 7, table 4-1) to the screw threads before and after final tightening.
c. Interface cable installation.
(1) Install the interface signal cable(s) (item 8, table 4-1 as described in TM 11-7440-239-15, AUTODIN DIGITAL SUBSCRIBER TERMINALS (STATION MANUAL), chapter 2, section IV
d. Control panel installation.
(1) Remove the blank panel (5 fig. 4-5) from the reference designation A6 area. Store the panel mounting screws and washers for future use in subparagraph h (18).


Figure 4-34. Partial routing of cables from control panel.
(2) Position the control panel assembly (fig. 4 6 and item 9 of table 4-1 face down in a servicing position in front of the mounting aperture.
(3) Route and clamp the cables as shown in figure 4-34
(4) Connect the two brown wires to TB-6 terminals $I$ and 2 as shown infigure 4-34
(5) Temporarily install the control panel assembly in its mounting aperture without using mounting hardware.
e. Relay and filter assembly installation. Refer to figures $4-35$ and $4-37$ and install the relay and filter assembly (24.4, fig. 4-5 and item 20, table 4-1] as follows:
(1) Disconnect the punched tape reader number one 11.5 VAC power wiring (twisted black and white wires) from the blower (21, fig. 4-5) terminal block (B1TB1, terminals I and 3). Extend the length of the black and white twisted pair by removing tie wraps for approximately one foot to release the looped portion. After the twisted pair is free, use tie wraps AMS17821-19 (item 17, table 4-1) to resecure punched tape reader number one cable. This twisted pair is identified as (D) in fifigures 4-35 and 4-37
(2) Connect the black and white wires (D) to relay K1 terminals 1 and 2 as shown in the wiring details in figure 4-35(detail A).
(3) Locate the six (6) wires broken out of cable (A) that are encased in sleeving (cable (C) in fig. 4-35 and 4-37). The six (6) wires consist of 2 pair of black and white twisted pair and 1 each brown and orange wire. Also locate the shortest set of black and white twisted pair wires and a green wire (cable ( F ) figures 4 35 and 4-37) from cable (A) and connect one lead (a) of an ohmmeter to the black wire.

Note. Cable (F) wires ir[|figures 4-35 and 4-37 are shown as not being encased in sleeving. However, on some paper tape readers the wires are covered with sleeving. Routing of the wires is the same whether encased in sleeving or not.
(4) Using the other lead (b) of the ohmmeter to verify continuity, locate the other end of the black wire in the six (6) wire cable and connect it to K1-7. Move meter lead (a) to the white wire in that cable. With meter lead (b) locate the white wire in the six (6) wire cable and connect it to K1-8 (fig. 4-35).
(5) Connect the black and white twisted pair and the green wire (F) to the blower (26, fig. 4-5) power terminal block as shown in figure 4-37
(6) Connect the remaining four wires encased in sleeving. (cable (C()) to relay KI terminals as shown in figure 4-35
(7) Clamp the cables to the relay bracket as shown in figure 4-35.
(8) Install the assembly in the enclosure as shown in figure 4-3.5. Tapped mounting holes are provided in the enclosure.
f. Filter assembly wiring.
(1) Locate the black and white twisted pair and green wire (three wires) broken off from cable (A) that are encased in sleeving.
(2) Connect this cable ((E), fig. 4-36 and clamp it to the filter assembly as shown in figure 4-36
g. Routing of cables in bottom of enclosure. Route and clamp the cables as shown irfigure 4-37.
h. Logic assembly installation.
(1) Route and clamp the four logic assembly cables to the enclosure structure as shown in figure 438. Leave the clamps loose enough to allow the cables to be slid back and forth through them.
(2) Remove the outer chassis slides and mounting hardware (part of 53, fig. 4-8) from the logic assembly (item 18,table 4-1.
(3) Install the outer slides inside the enclosure per figure 4-39 (holes are provided for mounting the slides in reference designation A4 area of the enclosure). Do not apply sealing compound to the screw threads at this time because it may be necessary to reposition the slides slightly for proper operation when the logic assembly is installed.
(4) Depress the slide stop catches (located midway along each of the top and bottom slides) and insert logic assembly A4 into the enclosure.
(5) With the logic assembly installed, reposition the outer slides, if necessary, and tighten screws. Apply sealing compound to the screw threads before and after final tightening.
(6) Pull the logic assembly A4 from the enclosure to its stop position.
(7) Remove printed circuit cards from locations A1 through A3 and A10 through A12 to improve access to the terminal blocks and to the cable clamps (installed in step 1) during final cable adjustments in steps 13 through 16.

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Figure 4-35. Relay assembly (K1) installation, exploded view.

note:

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Figure 4-36. Filter assembly (FL1) wiring details and cable routing.


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Figure 4-37. Routing of cables in bottom of enclosure and connections to blower.
(8) Connect wires to terminal blocks TB2 and TB3 as shown in figure 4-40.
(9) Connect cables to the logic assembly as shown below. Lock cable connectors in position as shown in detail A of figure 4-40.
Note. Make certain that the cables are not entangled so that they can be routed later as shown in figure 4-41.
(a) P3 (A4J4) to J4
(b) P 1 (A4J3) to J3
(c) $\mathrm{P} 2(\mathrm{~A} 4 \mathrm{~J} 2)$ to J 2
(d) P 1 (A4J1) to J1
(10) Clamp the cables as shown ih figure 4-40
(11) Being careful not to damage the cables, press the slide stop catches, slide the logic assembly into the enclosure and lock it into position.


Figure 4-38. Routing and clamping of logic assembly (A4) cables to enclosure.
(12) Route the cables around the rear edge of the logic assembly as shown in figure 4-41 and install the cable bar clamp.
(13) With the logic assembly locked in position, feed the excess cable through the upper cable clamps (installed in step 1) to the front of the enclosure.
(14) Swing the control panel clear and to the right to gain access to the cables with the logic assembly locked in the enclosure.
(15) From the rear of the enclosure, tighten the upper cable clamps then dress and bundle the cables using tie wraps as required.

Excess cable must be dressed in behind the control panel in such a manner as to be up and clear of the logic assembly and back and up to clear the front panel switches (see fig. 4-42).
(16) Unlock the logic assembly and slide it in and out several times to insure that the cables are free and that the cables cannot be fouled.
(17) Replace the printed circuit cards (removed in step 7) in locations Al through A3 and A10 through A12. (fig. 4-8).


NOTES:

1. APPLY SEALING COMPOUND SM-B-583244-008 TO SCREW THREADS BEFORE AND AFTER FINAL TIGTTENING.
2. ALL HARDWARE SHOWN IS SUPPLIED AS PART OF SLIDE.
. TOP SLIDE SHOWN, INSTALL LOWER SLIDE IN A SIMILAR MANNER.

Figure 4-39. Logic assembly slide installation details, exploded view.
(18) Install the control panel using the mounting hardware stored in sub-paragraph $d(1)$.
i. Power supply installation.
(1) Separate the inner parts of each slide from the middle and outer portions (item 29, table 4-1) and mounting hardware and install outer slide in the enclosure pe figure 4-43 (mounting holes are provided in reference designation PS2 area of enclosure). Do not apply sealing compound to screw threads at this time.
(2) Mount the inner slides on the power supply fiq. 4-10 and item 31, table 4-1) assembly as shown in figure 4-44
(3) If removed, reassemble the center slides to the inner slides which are attached to the power supply chassis.
(4) Insert the power supply assembly into the outer slides mounted in the enclosure.
(5) With the power supply in place, reposition the outer slides, if necessary; apply sealing compound on screw threads shown ir figure 4-43 before and after final tightening.
(6) Connect cable (B) (fig. 4-37) to power supply PS2 terminal board TBI as indicated in the following table:

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Table 4-2. Cable B Connections

| Wire color | PS2 termination | Voltage | Destination |
| :---: | :---: | :---: | :---: |
| Grey ---------------------------- | TB1 terminal 9*--------------- | 15 VAC ------------------------ | A6Z2-G. |
| Grey ---------------------------- | TB1 terminal 10* -------------- | 15 VAC ------------------------- | A6Z3-G. |
| Yellow -------------------------- | TB1 terminal 16 --------------- | +24 VDC ---------------------- | A6Z2-1-N.O. |
| White-yellow----------------- | TB1 terminal 17 --------------- | +24 VDC switched ----------- | A6Z2-1-Com. |

*Use ohmmeter to verify continuity between PS2 termination and destination.
(7) Connect cable (A) (fig. 4-37) to power supply PS2 terminal boards TB1 and TB2 as indicated in the following table. Use an ohmmeter to verify continuity between PS2 termination and destination.

Table 4-3. Cable A Connections

| Wire color | PS2 termination | Voltage | Destination |
| :---: | :---: | :---: | :---: |
| Black (jumper) -------------- | TB1 terminal 1---------------- | 120 VAC----------------------- | PS2 TB1 terminal 4. |
| Black -------------------------- | TB1 terminal 1---------------- | 120 VAC---------------------- | FL1 TB2 terminal 3. |
| White (jumper) -------------- | TB1 terminal 2---------------- | 120 VAC RTN---------------- | PS2 TB1 terminal 3. |
| White ------------------------- | TB1 terminal 2 | 120 VAC RTN--------------- | FL1 TB2 terminal 4. |
| White (jumper) --------------- | TB1 terminal 3 | Wire conn | ted above. |
| Black (jumper) -------------- | TB1 terminal 4---------------- | Wire conn | ted above. |
| Black --------------------------- | TB1 terminal 5----------------- | 120 VAC----------------------- | A5J2 pin U. |
| White | TB1 terminal 6 | 120 VAC RTN---------------- | A5J2 pin Y. |
| Black | TB1 terminal 7 | 120 VAC----------------------- | K1 pin 3. |
| White | TB1 terminal 8- | 120 VAC | K1 pin 4. |
| Green | TB1 terminal 15 --------------- | Hazard grd -------------------- | FL1 terminal E2. |
| Green -------------------------- | TB1 terminal 18 | Hazard grd -------------------- | A4 TB2 terminal 7. |
| Green -------------------------- | TB1 terminal 18 | Hazard grd -------------------- | A5J2 pin e. |
| Green | TB1 terminal 19 | Hazard grd -------------------- | BITB1 terminal 2. |
| Brown | TB1 terminal 21 --------------- | +4.5 VDC RTN--------------- | A4TB2, terminal 5. |
| Red ------------------------------ | TB2 terminal 2---------------- | +4.75 VDC -------------------- | A4TB3 terminal 2. |
| Orange------------------------ | TB2 terminal 3 | +12 VDC ---------------------- | K1 terminal 5. |
| Orange-------------------------- | TB2 terminal 3 | +12 VDC --------------------- | A4TB2 terminal 1. |
| Brown -------------------------- | TM2 terminal 4 | Com DC RTN ---------------- | Interface TB6 terminal 2. |
| Brown -------------------------- | TM2 terminal 4 ---------------- | Com DC RTN ---------------- | K1 terminal 6. |
| Blue------------------------------ | TB2 terminal 7---------------- | -12 VDC ------------------------ | A4TB2 terminal 2. |
| Violet ----------------------------------- | TB2 terminal 8- | -48 VDC ------------------------ | A4TB2 terminal 3. |
| Brown -------------------------- | TB2 terminal 9----------------- | -48 VDC RTN ---------------- | A4TB2 terminal 4. |

(8) Clamp the power supply cables to the rear bracket of the power supply as shown ir figure 4-45 (mounting holes are provided on the rear bracket).
(9) Use tie wrap MS17821-1-9 (item 17, table 4-1) to bind excess cable as shown in figure 4-45
j. Validation of cable routing. While observing the cables from the rear of the enclosure, pull out and close reader mechanism A5, logic assembly A4, and power supply PS2 to insure that the cables are not binding. If cables are catching, readjust cable clamps and use tie wraps to eliminate the trouble.
k. Power reconnection. Reconnect the input power cable to filter assembly FL1 TB1 (21, fig. 4-5). Turn on ac power to the punched tape reader.
I. Changing reference designation plate. Remove the single punched tape reader reference designation plate from the inside of the right front enclosure door by pulling it off.

Clean adhesive residue from area before replacing it with a dual reader reference designation plate (item 34, table 4-1.
m. Initial turn-on and checkout.
(1) Initial turn-on. Perform turn-on procedures outlined in daragraphs 3-1 and 3-2d, TM11-7440-239-15, AUTODIN Digital Subscriber Terminals (Station Manual).
(2) Self-test checkout procedures. Perform the self-test checkout procedures outlined in subparagraphs 3-3a and 3-3f, TM 11-7440-239-15.
(3) Back-to-back mode tests. Perform the back-to-back mode checkout procedures outlined in paragraph 3-5 TM 11-7440-239-15.
(4) On-line tests. Perform the on-line checkout procedures outlined in paragraph 3-6, TM 11-7440-23915.
n. Secure enclosure. Replace the rear panel on the enclosure.

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Figure 4-40. Logic assembly (A4) connections and cable clamping.


NOTE:


Figure 4-41. Routing and clamping of cables to rear of logic assembly (A4).


Figure 4-42. Dressing of excess cable behind control panel.


NOTES:

1. APPLY SEALING COMPOUND SM-8-58324-00 TO SCREW THREADS BEFORE AND AFTER FINAL TIGHTENING.
2. USE ITEMS 45, AND 30 TABLE 4-1 TO SECURE SLIDES TO REAR OF ENCLOSURE IN PLACE OF HARDWARE FURNISHED WITH SLIDE. ALL OTHER SLIDE.
3. RIGHT HAND SLIDE SHOWN. INSTALL LETT HAND SLIDE in a similar mañer.

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Figure 4-43. Power supply outer slide installation details, exploded view.


NOTES:

1. LEFT HAND INNER SLIDE SHOWN. MOUNT RIGHT HAND SLIDE IN A SIMILAR MANNER.
2. ON SLI DES USING BUTION TYPE LATCHES, THE SPRING AND FLAT WASHER ARE NOT USED.
3. MOUNTING HOLES ARE PROVIDED ON THE POWER SUPPLY ASSEMBLY.
4. ALL HARDWARE SHOWN IS FURNI SHED AS PART OF SLIDE.

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Figure 4-44. Mounting of inner slide to power supply (PS2).


Figure 4-45. Clamping of cables to power supply (PS2).

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## Section VIII. TRANSMISSION IDENTIFICATION GENERATOR KIT MK-1 583/G INSTALLATION

## 4-70. General

a. Scope. This section contains the parts list, step-by-step installation procedures and checkout procedures required to install the transmission identification generator (TIG) kit MK-1583/G in the punched tape reader locations A7 and/or A8.
b. Power. For safety, it is imperative that the power to the punched tape reader be turned off during installation of the conversion kit.

Thus, the DSTE tape send channel must be off-line during the conversion.
c. Manpower Required. To prevent damage to equipment and injury to personnel, two men will be required to perform the conversion.

4-71. Tools, Materials and Test Equipment Required
a. Tools and Test Equipment. The following recommended tools and test equipment (or equal) are required for installation of the TIG conversion kit:

| Item Description | Part number | FSN | Quantity |
| :---: | :---: | :---: | :---: |
| Toolkit, electronic equipment | TK-105 | 5186-610-8177 | 1 |
| Toolkit, general (AUTODIN DST) |  |  | 1 |
| Drill, electric, portable, $3 / 8$-inch chuck capacity. |  | ------ | 1 |
| Drill bit, 3,/32-inch diameter |  |  | 1 |
| Drill bit, 3./16 inch diameter |  |  | 1 |
| Drill bit, 1/8-inch diameter | ---------------------------- |  | 1 |
| Drill bit, 3 '8-inch diameter |  |  | 1 |
| Knockout driver, hydraulic | Greenlee No. 7646-A-- |  | 1 |
| Punch die, 3,/4-inch round | Greenlee ----------------- |  | 1 |
| Punch die, 1 1/2-inch round | Greenlee ----------------- |  | 1 |
| Extender, printed circuit board | General Dynamics No. 809002-876. |  | 1 |
| Multimeter AN,/USM-210 | Simpson Model 260-5. | 6625-149-6301 ------------ | 1 |
| Voltmeter, Digital (or equivalent with accuracy of +005 volt). | Non-linear Systems Inc Model X-1/5. | 6625-168-0669 ------------- | 1 |
| Oscilloscope AN/USM-309(V)I consists of: | Hewlett-Packard --------- | 6625-121-63281----------- | 1 |
| Oscilloscope | Model 140A |  |  |
| Generator | Model 1421A |  |  |
| Amplifier | Model H06-1405A |  |  |
| Test Prods (2 ea) | No. C16-10003B |  |  |
| Probe tip, coil spring | Textronix <br> No. 206-0061-00 | 6625-054-02312------------ | 2 |
| Cart, oscilloscope | Hewlett-Packard1 model 1119B. | --- | 1 |
| Cleaner, vacuum, hand type | Ideal Mfg. Co. No. 22-113 | 7910-250-8039 ------------ | 1 |

b. Materials. The following materials are required for installation of the TIG conversion kit:
(1) Solder, lead-tin alloy (60,/40), rosin core, 1/32-inch diameter.
(2) Installation assembly, transmission identification generator kit MK-1583/G, General Dynamics Electro Dynamics Division part No. 00001498. Table 4-4 lists the parts contained in the installation kit.

Table 4-4. Parts List for Transmission Identification Generator Kit MK-1583/G

| Item No. | Qty. | U/M | Part number | Item description |
| :--- | :--- | :--- | :--- | :--- |
| 1 | 1 | EA | ${ }^{*} 00-001509$ | Special purpose electrical cable assembly (EM signal). |
| 2 | 1 | EA | ${ }^{*} 00-001497$ | Special purpose electrical cable assembly (TIG to TIG). |
| 3 | 1 | EA | ${ }^{*} 00-001501$ | Electrical equipment chassis assembly (A7 or A8). |
| 4 | 1 | EA | ${ }^{*} 12-890081$ | Control logic assembly (PC card A1A2 or A4A2). |

Table 4-4. Parts List for Transmission Identification Generator Kit MK-158./G-Continued

| Item No. | Qty. | U/M | Part number | Item description |
| :---: | :---: | :---: | :---: | :---: |
| 5 | 80 | FT | SMB546288-444 | Electrical wire |
| 6 | 16 | EA | MS17821-1-9 | Adjustable cable strap |
| 7 | 1 | EA | *540205-109 | Nylon cable clamp |
| 8 | 1 | EA | *540205-120 | Nylon cable clamp |
| 9 | 2 | EA | SMC546215-2 | Polarizing key (connector) |
| 10 | 1 | EA | *04-001348 | Extraction hand tool |
| 11 | 1 | EA | SMC546215-1 | PC card insulator (XA1A2 or XA4A2). |
| 12 | 2 | EA | MS51957-27 | Screw, panhead, No. 6-32, 5/16 in. long. |
| 13 | 2 | EA | MS35338-136 | Lockwasher, split, No. 6 |
| 14 | 2 | EA | AN960C6L | Washer, flat, No. 6. |
| 15 | 4 | EA | MS51958-63 | Screw, panhead, No. 10-32, 1/2 in. long. |
| 16 | 4 | EA | MS35650-304 | Nut, hexagon, No. 10-32 |
| 17 | 4 | EA | MS35338-138 | Lockwasher, split, No. 10 |
| 18 | 8 | EA | AN960C10 | Washer, flat, No. 10 |
| 19 | 6.28 | IN | MS21266-2N | Plastic grommet, edging |
| 20 | 1 | EA | *04-001345-1 | Adhesive |
| 21 | 1 | EA | *00-001551 | TIG kit repair parts list |
| 22 | 1 | EA | *01-002851 | Reference designation plate |
| 23 | 2 | EA | *04-001337 | Cable tie mounting device |
| 24 | 2 | EA | MS51959-18 | Screw, flathead. No. 4-40, 5/8 in. long |
| 25 | 2 | EA | MS35949-244 | Nut, hexagon, No. 4-40 |
| 26 | 2 | EA | MS35338-135 | Lockwasher, No. 4 |
| 27 | 2 | EA | AN960C4L | Washer, flat, No. 4 |
| 28 | 1 | EA | *540205-112 | Nylon cable clamp |
| 29 | 1 | EA | SM-E-546543 | Output deselect (PC card CCU A1A30) |

*General Dynamics, Electro Dynamics Division part number.

## 4-72. Installation Procedure

a. Preliminary Procedure.
(1) Check the conversion kit parts against the parts list table 4-4 to verify that all of the necessary parts are contained in the kit.
(2) Read the entire installation procedure outlined in baragraphs 4-70 through 4-72 before installing the TIG.
(3) Store TIG kit repair parts list (item 21,table 4-4 with appendix D for use in the logistics support of TIG until such time as these parts have been formally incorporated in the repair part and special tools list.
(4) For safety, disconnect the 120 volts ac power to the punched tape reader.
(5) Remove the top rear panel (72, fig. 4-5 from the punched tape reader. Identify and retain the mounting hardware (69, 70, and 71) for use in replacement of the panel after completion of the conversion.
(6) Determine if the TIG is to be installed in the A7 or in the A8 assembly location on the punched tape reader. If you are installing the TIG in the A7 location (6, fig. 4-47), references made in the following paragraphs will be to punched tape reader number 1 interface plate assembly, logic assembly AI, and power supply PS1.

If you are installing the TIG assembly in the A8 location (7, fig. 4-47), then the references in the following paragraphs will be to the punched tape reader number 2 interface plate assembly, logic assembly A4, and power supply PS2.
b. Reference Designation Plate. Take the reference designation plate (item 22 table 4-4) from the kit parts and-
(1) If installing a dual TIG kit in both the A7 and A8 locations, remove the protective covering and press into place above existing reference designation plate on the inside of the right front door as shown by item 1 of figure 4-47
(2) If installing only one TIG assembly, cut the reference designation plate on the line between A7 and A8 and discard the half that will not be installed. Then, removing the protective covering, press into proper place above the existing reference designation plate on the inside of the right front door as shown by item 1, offfigure 4-47.
c. Modification of Logic Assembly A1 (or A4). It is not recommended that the logic assembly be removed from the punched tape reader inclosure to perform the following modifications. It will be necessary, however, to depress the slide stop catches to allow the logic assembly to be withdrawn further from the cabinet to make the wire wrap connections to be added connector J 1 and J4 terminals.

Exercise caution that the logic assembly is not pulled so far out of the inclosure that it is no longer supported by the slides.
(1) Tale the PC card insulator (item 11, table 44) and identify one end of the insulator contacts as terminal 1. Then install the two insulator polarizing keys (item 9, table 4-4) between pins 3 and 4 and between pins 18 and 19. Use a small amount of adhesive (item 20, table 1-4) to secure the polarizing keys, but insure the adhesive does not flow onto the insulator contact pins.
(2) Install the PC card insulator in the logic assembly A2 location. Insure the insulator contact identified as pin I in (1) above is placed at the top of the logic assembly chassis. Secure the insulator (24, fig. 447) using two No. $632,5 / 16$-inch long panhead screws (item 12, table 4-4. two No. 6 lockwashers (item 13), and two No. 6 flat washers (item 14) as shown onfigure 4-47(items 21, 22, and 23).

## CAUTION

Extreme care must be taken in performing the backplane wiring modifications in the following steps. Any error in wiring will result in improper operation. In addition, damage to equipment is possible when power is applied. Before removing a wire, first mark both contact pins, then verify continuity with an ohmmeter. In a similar manner, verify continuity between terminals for each added wire. In locating a terminal, always double check first to insure the proper connector or jack location has been selected and then double check that the proper pin on that connector or jack has been identified.
(3) Remove the following wires from the logic assembly backplane:

| From- | To- |
| :---: | :---: |
| XA05-10-------------------- | XA15-16 |
| XA05-14 --------------------- | XA14-6 |
| XA05-W -------------------- | XA06-15 |
| XA05-Y --------------------- | XA06-W |
| XA05-Z --------------------- | XA06-X |
| XA05-21 -------------------- | XA06-T |
| XA05-E ---------------------- | XA06-18 |
| XA05-K ---------------------- | XA06-5 |
| From- | To- |
| XA05-L---------------------- | XA06-23 |
| XA05-7----------------------- | XA07-16 |
| XA15-D ---------------------- | XA16-H |

(4) Using wire (item 5, table 44), add the following wires to the logic assembly backplane. Route the wires in a square path similar to existing wiring in the backplane. In addition, in the case of the longer wires, route the new wire under existing wiring at approximately 4 - to 6 -inch intervals to hold the wiring flush against the logic assembly chassis.

| From- | To- |
| :---: | :---: |
| J01-A ------------------------ | XA02-13 |
| J04-A ------------------------- | XA02-A |
| J04-E ------------------------- | XA02-N |
| J04-J------------------------- -- -- | XA02-18 |
| J04-01----------------------- -- -- | XA02-A |
| J04-03--------------------- | XA04-09 |
| J04-06 | XA02-B |
| J04-09-- | J04-11 |
| J02-14 | J04-13 |
| XA01-T------------------ | XA02-D |
| XA02-E------------------- | XA05-14 |
| XA02-K-------------------- | XA04-18 |
| XA02-V------------------- | XA06-T |
| XA02-Z--------------------- | XA05-E |
| XA02-02 --------------------- | XA04-B |
| XA02-05 --------------------- | XA14-06 |
| XA02-16 ----------------- | XA06-W |
| XA02-20 ----------------- | XA05-W |
| XA02-23 --------------------- | XA05-Z |
| XA02-10 --------------------- | XA07-16 |
| J01-B ------------------------ | J04-P |
| J04-B ------------------------ | XA02-M |
| J04-F ------------------------- | XA02-R |
| J04-K ------------------------- | XA02-W |
| J04-02------------------------ | XA02-01 |
| J04-04----------------------- | XA02-14 |
| J04-07-------------- | XA02-02 |
| J04-11---------------------- | J04-15 |
| J04-14-- | XA01-14 |
| XA01-01 | XA02-A |
| XA02-F-- | XA15-16 |
| XA02-T-- | XA06-23 |
| XA02-X-- | XA05-Y |
| XA02-AA------------------ | XA05-07 |
| XA02-03 -------------------- | XA03-03 |
| XA02-09 ------------------- | KA14-10 |
| XA02-17 --------------------- | KA06-05 |
| XA02-21 -------------------- | XA05-K |
| XA02-06 --------------------- | XA15-D |
| XA02-F---------------------- | XA02-L |
| J02-14----------------------- | XA03-01 |
| J04-D ------------------------- | XA02-P |
| J04-H ------------------------ | XA02-S |
| J04-03----------------------- | XA02-01 |
| J04-05----------------------- | XA02-06 |
| J04-07------------------------- | J04-08 |
| J04-12---------------------- | J04-13 |


| From- | To- |
| :---: | :---: |
| XA01-B ---------------------- | XA02-B |
| XA02-C ---------------------- | XA03-C |
| XA02-H -------------------- | XA04-06 |
| XA02-U ----------------------- | XA06-18 |
| XA02-Y ----------------------- | XA05-L |
| XA02-01 ------------------- | XA03-A |
| XA02-04 ------------------- | XA04-D |
| XA02-15-------------------- | XA06-15 |
| XA02-19 --------------------- | XA06-X |
| XA02-22---------------------- | XA05-21 |
| XA02-11 -------------------- | XA02-AA |

d. Logic Assembly Wiring Checkout Procedures.

## NOTE

Do not install the new PC card A2 into the logic assembly until after the following voltage checks have been completed.
(1) Apply 120 VAC power to the punched tape reader chassis.
(2) Depress the AC POWER switch on the punched tape reader. Observe the AC POWER and the DC POWER indicators light white.
(3) Use a voltmeter and check following approximate voltages to groundpoint XA1-A:

| Test point | Voltage |
| :---: | :---: |
| XA2-1 ------------------------ | 0 volt |
| XA2-A ------------------------- | 0 volt |
| XA2-2 ------------------------ | +4.75 volts |
| XA2-B ----------------------- | +4.75 volts |
| XA2-3 ----------------------- | - 12 volts |
| XA2-C------------------------ | + 12 volts |
| J04-1 ------------------------- | 0 volt |
| J04-2 ------------------------- | 0 volt |
| J04-3 ------------------------ | 0 volt |
| J04-9 ------------------------- | 0 volt |
| J04-11 ---------------------- | 0 volt |
| J04-12 ----------------------- | 0 volt |
| J04-13 ----------------------- | 0 volt |
| J04-15 ---------------------- | 0 volt |
| J04-6 ------------------------- | +4.75 volts |
| J04-7 -------------------------- | +4.75 volts |
| J04-8 ------------------------ | +4.75 volts |

(4) Use a voltmeter and check the voltage between all terminals on XA2 to groundpoint XA1-A. With the exception of terminals XA2-3 and XA2-C (-12 VDC and +12 VDC respectively), all of the terminals should read between 0 volt and +4.75 volts.
(5) Using a digital voltmeter, check power supply output voltages as outlined in paragraph 4-63. Adjust power supply output voltages if required.
(6) Depress the AC POWER switch indicator on the punched tape reader.

Check to insure the AC POWER and the DC POWER indicators are not illuminated.
(7) Install PC card A2 (item 4 table 4-4) in the logic assembly.
(8) Install a temporary jumper wire between terminals XA2-A and XA2-M. This wire functions to force the TIG control logic PC card A2 into the off-line mode.
(9) Depress the AC POWER switch indicator on the punched tape reader. Observe that the AC POWER, DC POWER, and STOP indicators are illuminated.
(10) Check the punched tape reader for proper operation in local test mode by following procedures outlined in baragraphs 2-2 through 2-8
(11) Perform back-to-back mode test of the punched tape reader, through the CCU, to the paper tape punch. Verify that the punched tape reader operates in a normal manner without faults and the message punched by the receive device is identical to the transmitted message from the punched tape reader. Procedures outlined in paragraph 3-5 TM 11-7440-23915 , may be used as a guide to operating other terminal equipment.

## NOTE

At this point in the installation procedure of the TIG assembly, it is possible to place the punched tape reader back in the on-line mode. Then, complete the installation of the TIG assembly at a later time.
e. Preliminary Procedure for Final Step of Installation.
(1) Remove AC POWER from the punched tape reader unit.
(2) Remove PC cards AI through A5 (items 1, 2,3 or 3.1, and 4 or 4.1, fig. 4-8 and 26, fig. 4-47) from the logic assembly AI or A4 of the punched tape reader being modified. Identify each card removed to insure proper replacement at a later date.
(3) Remove the temporary jumper wire from terminals XA2-A to XA2-M.

## f. Printed Circuit Card A2 Strapping Options.

During initial installation, several solder type hard-wire strapping options must be made on the PC card to be installed in the logic assembly A1A2 or A4A2 location. The message start position strapping board determination if the TI sequence begins with the 1st, 2nd, 3d, or 4th character of the TI forma (para 3-84b).

The channel designator strapping board generates the three alphabetical characters identifying the terminal that are transmitted as the 5th, 6th, and 7th characters of the TI format. Use wire (item 5, table 4-4 to make the strap on PC card A2. Strip insulation from this wire prior to making connections. These straps are described below.
(1) Determine the message start character position assigned to the terminal.
(2) Refer to figure 4-4\$. 1 and identify the four terminals used for the message start position strapping board.
(3) Solder strapping wires from terminals $2^{\circ}$ and $2^{\prime}$ to terminals 0 and 1 as follows:

| Start position |  | Strap connections |
| :---: | :---: | :---: |
| First character position | TI format transmitted |  |
| 1 | ZCZC THROUGH NUL | $\begin{aligned} & 2^{\circ} \text { TO } 0 \text { and } 2^{\prime} \\ & \text { TO O } \end{aligned}$ |
| 2 | CZC THROUGH NUL | $\begin{aligned} & 2^{\circ} \text { TO } 1 \text { and } 2^{\prime} \\ & \text { TO } 0 \end{aligned}$ |
| 3 | ZC TROUGH NUL | $\begin{aligned} & 2^{\circ} \text { TO } 0 \text { and } 2^{\prime} \\ & \text { TO } 1 \end{aligned}$ |
| 4 | C THROUGH NUL | None |

(4) Determine the three alphabetical characters that are assigned as channel designation characters to identify the terminal.
(5) Refer to figure 3-3 and determine the ASCII code for columns 1 through 7 to be used on each of the three channel designation characters.
(6) Refer to figure 4-45 1 and locate the 35 terminals used in the channel designator strapping board. The seven terminals 1A through 7A are used as a strap options for the first channel designator character. Terminals B1 through 7B are strap options for the second character and terminals 1C through 7C are used for the third character. Make a solder-type hard-wire strap from these 21 terminals to the nearest terminal 0 or 1 terminal depending upon the ASCII code for each bit of the three characters. Terminal 1A should be connected as indicated in column 1 of chart in figure 3-3 for the character used as the first channel designation character. In a similar manner, make the remaining strap connections by relating the numerical portion of the PC card A2 terminal identification to the column number shown in figure 3-3.
g. Installing TIG Chassis.
(1) Remove the cover (2 fig. 4-48) from the TIG assembly by removing the four flathead screws (1).


CHANNEL DESIGNATER STRAPPING
BOARD

Figure 4-45.1. PC card A2 strapping options.
(2) Place the TIG assembly chassis in the proper position on the top of the punched tape reader inclosure as shown in figure 4-46. Position the TIG chassis flush with the rear of the punched tape reader inclosure, the blue painted portion of the TIG chassis $1 / 2$ inch from the side.
(3) Using a pencil or a scribe, mark the position of all five holes of the TIG chassis on the top of the punched tape reader inclosure.
(4) Remove the TIG chassis and center punch all five holes.
(5) Place protective covering material such as plastic or cloth under the top of the punched tape reader inclosure to prevent metal chips from getting into the punched tape reader mechanism, logic assembly, and power supply.
(6) Drill a $3 / 32$-inch pilot hole in all five holes marked on the punched tape reader inclosure.
(7) Using a $3 / 16$-inch drill bit, enlarge the four mounting holes.
(8) Using a $3 / 8$-inch drill bit, drill the center hole to be used as a guide for the knockout punch.
(9) Insert a $3 / 4$-inch round punch die into the hydraulic knockout driver and punch out a $3 / 4$-inch hole.
(10) Remove the $3 / 4$-inch die and insert a $11 / 2$-inch round die in the hydraulic knockout driver. Use the $3 / 4$-inch hole made in previous step as a pilot and punch out a 11/2-inch hole. Remove any burrs from the hole.
(11) Locate the two vertical angle supports running along either side of the punched tape reader inclosure. Take a cable tie mounting device (item 23 ,table 4-4 and position the mounting device flush with the top of the angle support as shown by item 17,figure $4-47$. Using a pencil or scribe, mark the position of the hole in the center of the mounting device on the angle bracket.
(12) Center punch the hole marked in preceding step and drill a $1 / 8$-inch diameter hole in the angle bracket.
(13) Using one each No. 4-40 flathead screw, No. 4-40 hex nut, No. 4 lockwasher, and No. 4 flat washer (items 24 through 27, table 4-4], remove the protective covering and mount the cable tie mounting device to the punched tape reader inclosure angle bracket. Insure the cable tie mounting device is on the front side of the


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Figure 4-46. TIG chassis position.
Change 4 4-65


Figure 4-47. Transmission identification generator kit, component location diagram.

## TM 11-7440-219-15/NAVSHIPS 0967-324-0054/TO 31W4-2G-61

```
Reference designation plate
Nut, hex, No 10-32
Lockwasher. No. 10
4 Washer, flat, No. 10
5 Screw, panhead, No. 10-32, 5/16
    in. long
6 TIG assembly A7
7 TIG assembly A8
8 Cable strap
9 Cable clamp
10 TIG cable assembly
11 Nut, hex, No. 4-40
```

12 Lockwasher, No. 4
13 Washer, flat, No. 4
14 Screw, flathead, No. 4-40, 5/8 in. long
15 Cable clamp
16 EM signal cable assembly
17 Cable tie mounting device
18 TIG to TIG cable assembly
19 Cable tie mounting device
20 Cable clamp
21 Screw panhead, No. 6-32, 5/16 in. long
Figure 4-47-Continued.

22 Washer, flat, No. 6
23 Lockwasher, No. 6
24 PC card insulator
25 Polarizing key
26 PC card (A1A2)
27 Grommet
28 Terminal lug
29 Electrical contact pin
30 Identification plate
31 Terminal lug
32 Terminal lug
angle bracket with the hex nut and washers to the rear of the enclosure.
(14) Take the plastic grommet (item 19, table 4-4 and place it in the $11 / 2$-inch hole to verify proper length. If necessary, trim the end of the grommet to insure a snug fit in the hole. Remove the grommet.
(15) Apply adhesive (item 20,table 4-4) to the portion of the grommet that will be in contact with the metal portion of the reader enclosure and then place the grommet into the $11 / 2$ inch hole in the top of the punched tape reader.
(16) Feed the cable attached to the TIG assembly chassis through the large hole in the top of the enclosure and position the TIG assembly chassis in place. Secure by using the 4 panhead screws, 4 nuts, 4 lockwashers, and 8 washers (items 15 through 18, table 4-4). Position the hardware as shown ir figure 4-47 (items 2, 3, 4, and 5).
(17) Remove the bottom cable clamp (124, Detail E, I, or L, fig. 4-5) from the inside rear of the logic assembly chassis. This is the cable clamp that secures the cable routed to TB2, TB3, and J4. Retain the hardware for later replacement.
(18) Disconnect the contact assembly plugged into J4. In the case of the single punched tape reader, this contact assembly is identified as item 40, figure 45, detail E. In the case of dual punched tape reader units, the contact assembly in the logic assembly Al is identified as item 42 in figure 45 , detail I and the contact assembly in the logic assembly A4 is identified as 46 , in figure $4-5$. detail L .
(19) Remove the cable bar clamp (130 fig. 4-5) by removing two nuts (127), two lockwashers (128), and two washers (129) from the rear of the logic assembly being modified. Retain the cable bar clamp and hardware for later replacement.
(20) Route the TIG assembly cable (10 fig. 4-47) in the following manner (fig. 4-47):
(a) From the TIG assembly chassis to the cable tie mounting device (17, fig. 447 ).
(b) Follow the punched tape reader angle bracket down to the top rear of the interface plate and then forward to the top front of the interface plate.
(c) From the above point, the TIG assembly cable should follow the four cables going to logic assembly.
(d) Cable should then be routed so electrical contacts can be inserted into the contact assembly plugged into A1J4 or A4J4. See (18) above for identification of contact assembly.
(21) Insert the electrical contact pins on the end of each wire into the contact assembly identified in (20) above. Press each pin into its appropriate socket until an audible click is heard. The electrical contact removal tool (item 10, table 4-4) is provided in case of error. To remove a contact, insert the removal tool as far as it will go into the contact assembly from the side opposite of the wire. Grasp the wire and pull it out and then remove the removal tool. The following identifies the placement of each wire into the contact assembly:

| WIRE COLOR | PS (A1J4 or A4J4) |
| :--- | :--- |
| termination |  |

(22) Open the front panel of the TIG assembly to gain access to TIG assembly switch S1 and PC card AI. Use an ohmmeter and verify accuracy of previous step by measuring continuity between the following points:

| Contact assembly <br> P3 (A1J4 or A4J4) <br> terminal | TIG assembly <br> A7 or A8 terminal |
| :---: | :---: |
| 1 | A1E7 |
| 2 | A1E8 |
| 3 | A1E9 |
| 4 | A1E13 |
| 5 | ALE14 |
| 6 | A1E10 |
| 7 | A1E11 |
| 8 | S1-3 |
| 9 | S1-1 |
| 13 | S1-5 |
| 14 | A1E15 |
| A | A1E6 |
| B | S1-2 |
| D | A1E19 |
| E | A1E18 |
| F | A1E16 |
| H | A1E17 |
| J | A1E20 |
| P | DS1-C |

(23) Secure the TIG assembly cable (10, fig. 4-47) to the contact assembly as shown in detail C of figure 4-47. Use one cable clamp (item 7 table 4-4) and hardware consisting of one each No. 4-40 flathead screw (item 24), No. 4-40 hex nut (item 25), flat washer (item 27), and lockwasher (item 26).
(24) Secure the cables routed to logic assembly TB2, TB3, and J4 with cable clamp (20, fig. 447). Use the cable clamp (item 8 table 4-4) and the hardware removed from this location in a previous step.
(25) Complete securing of the TIG assembly cable by proceeding in the following manner:
(a) Refer to detail A of figure 4-47 and remove the hardware holding the end cable clamp. Install cable clamp (item 28,table 4-4) as shown in figure 4-47(item 9) and replace hardware to secure both cable clamps. Push the logic assembly to its closed position. Replace cable bar ( 130 fig. 4-5) to hold all cables. Do not tighten hex nuts (127) at this time.
(b) Use cable straps (item 6, table 4-
4) and tie the TIG assembly cable to the other cables at two different points between the cable clamp installed in (a) above and the logic assembly.
(c) Using one cable strap (8, fig. 447), secure the TIG assembly cable (10) to the cable tie mount (17) previously installed.
(d) Pull the logic assembly to its open position.
(e) Use cable straps to secure the TIG assembly cable to the angle bracket and the reader mechanism cables to the top front of the interface plate assembly. Place the cable straps at 10 to 15 -inch intervals.
(f) Use cable straps as required between the cable clamp cluster (detail A, fig. P47) and the top front corner of the interface plate assembly to prevent any cable from interfering with logic assembly slide operation. Excess cable length should be secured at this point.
(26) Disconnect the remaining contact assemblies plugged into the logic assembly being modified.
(27) Take the EM signal cable assembly (item 1, table 4-4] and use an ohmmeter to measure continuity to determine which electrical contact is connected to the longest white wire. Take this wire and insert it into terminal B of the contact assembly to be connected to the A1JI or A4J1 connector.
(28) Take the second wire in the EM signal cable assembly and insert its contact pin into the insulator for terminal A of the same contact assembly.
(29) Secure the EM signal cable assembly to the contact assembly by removing the cable clamp (58, fig. 4-5) from the contact assembly and then replacing it so that the cable clamp secures both cables.
(30) Replace all four contact assemblies into their proper connector. Also replace PC cards AI through A5.
(31) Secure the EM signal cable assembly to the inside rear of the logic assembly chassis by removing the top cable clamp (121, fig. 45) and then replacing the cable clamp to secure both cables.
(32) Route the EM signal cable (16, fig. 447) in the same path as the other cable connected to the contact assembly A1J1 (or A4J1) to the interface control panel.
(33) Secure the cable by removing the cable clamp (detail A,fig. 4-47) and replacing the cable clamp to hold both cables.
(34) Use cable straps (item 6, table 4-4 and tie the EM signal cable to the adjacent cables
at two different points between the cable clamp installed in (33) above and the logic assembly.
(35) Tighten the hardware (127, 128, and 129, fig. 4-5) holding cable bar clamp (130). Insure all cables to the logic assembly are securely held by the cable bar clamp.
(36) Route the short lead of the EM signal cable to the interface plate assembly and connect the white wire to terminal board TB2 (or TB5), terminal 9. Connect the black wire to terminal board TB2 (or TB5), terminal 10.
(37) Route the long lead of the EM signal cable to the power supply by following the path of the other power cables. Connect the white wire to the power supply (PS1 for the A7 assembly; PS2 for the A8 assembly) terminal board TB1, terminal 9. Connect the black wire to the power supply terminal board TB1, terminal 19.
(38) Complete securing of the EM signal cable by using cable straps (item 6. table 4-4) at 8 to 10inch intervals to tie the EM signal cable to adjacent cables. Insure excess length of the cable is looped on the floor of the punched tape reader enclosure.
h. Dual TIG Installation Interconnection. In those installations having dual TIG assemblies A7 and A8 both installed, the TIG to TIG interconnecting cable assembly (item 2 table 4-4) may be optional. Install this cable in the following manner:

## NOTE

> In single TIG installations this cable is not used. Also, in dual TIG installations there will be an excess TIG to TIG cable assembly since the cable is furnished as a part of both TIG modification kits. Discard excess cable(s).
(1) Attach the end of the cable having five terminal lugs to the terminal board TB1 in the TIG assembly A7. Make the connections to terminal board A7TB1 as follows

| Wire | Termination |
| :---: | :---: |
| BLACK. | A7TB1-8 |
| RED ........................................... | A7TB1-7 |
| WHITE ......................................... | A7TB1-5 |
| BLUE | A7TB1-4 |
| BLACK (SHIELD)........................... | A7TB1-6 |

(2) Route cable (item 18) as shown on figure 447 from the A7 assembly, through the punched tape
reader enclosure, to the A8 assembly. Connect the four terminals to A8TB1 as follows:

| Wire | Termination |
| :---: | :---: |
| BLACK. | A8TB1-5 |
| RED. | A8TB11-4 |
| WHITE | A8TR1-8 |
| BLUE ............ | A8TB1-7 |

(3) Attach two (one supplied as a part of each TIG modification kit) cable tie mounting devices (item 23, table 4-4) to the inside top of the punched tape reader enclosure as shown by item 19 or figure 4-47. These mounting devices should be placed approximately 4 to 5 inches from the holes in the top of the punched tape reader enclosure and positioned so a cable tie can be fed through the mounting device and around the TIG to TIG cable assembly (18 fig. 4-47).
(4) Position the TIG to TIG cable assembly so an equal amount of excess cable is looped in each TIG assembly and then secure the cable by using four cable straps (item 6, table 4-4) tying the cable to the two mounting devices (5 fig. 4-48) inside the TIG chassis and the two mounting devices installed in the preceding step.
i. Replace the TIG cover (2, fig. 4-47) with the four flathead screws (1).
$j$. Not used.
k. At the common control unit, open the righthand front door, pull out the logic assembly AI, and remove PC card A30 (26, fig. 4-6. TM 117440-214-15).
l. Take the new CCU PC card A1A30 (item 29, table/part No. SM-E-546543) and insert it into the CCU A1A30 location.
m. Retain the old CCU PC card A1A30 (part No. SM-E-546581) for future replacement into the common control unit should the TIG kit be removed from the punched tape reader or the common control unit returned to the depot.
n. Secure the common control unit, by closing the logic assembly Al and shutting the right-hand front door.

## 4-73. Initial Turn-On and Checkout

a. Initial Turn-On.
(1) Visually inspect the punched tape reader and the TIG kit to insure there are no loose or shorted wires, tools left in the equipment, or other condition which might cause damage when power is applied.
(2) Restore the 120 VAC power to the punched tape reader cabinet.
(3) Perform initial turn-on procedures outlined in paragraph 3-2d, AUTODIN Digital Subscriber Terminals (Station Manual).
(4) Place the TIG ON-LINE/OFF-LINE switch in the ON-LINE position. Check that the TIG ON indicator lights white. Check that the TIG Channel Sequence Number NEXT NUMBER indicators display 000.
(5) Set the TIG MANUAL UPDATE thumbwheel switches to 111 and then depress the LOAD switch. Check that the TIG Channel Sequence Number NEXT NUMBER indicators display 111.
(6) Using the same procedure as outlined in preceding paragraph, check the loading of 222, 333, $444,555,666,777,888,999$, and 000.
(7) Place the TIG ON-LINE/OFF-LINE switch in the OFF-LINE position. Check that the TIG ON indicator is not lighted. Check that the TIG channel sequence number NEXT NUMBER indicators display 000 (the last number loaded into the channel sequence circuitry).
b. Checkout Procedure, Reader, Punched Tape RP-154(P)/G. Perform the following checkout procedures on the punched tape reader with the TIG in the off-line mode:
(1) Perform the punched tape reader selftest checkout procedures outlined in paragraphs 3-3k and TM 11-7440-239-15.
(2) Perform the back-to-back mode checkout procedures applicable to punched tape reader operation outlined in paragraph 3-5. TM 117440-239-15.
(3) Perform the on-line checkout procedures applicable to punched tape reader operation outlined in paragraph 3-6, TM 11-7440-239-15.
c. Self-Test Checkout Procedure, Transmission Identification Generator MK-1583/,G (TIG).
(1) Place the TIG ON-LINE/OFF-LINE switch in the ON-LINE position. Check that the TIG ON indicator illuminates.
(2) Perform the punched tape reader selftest checkout procedures outlined in paragraphs 3-3k and $3 f$, TM 11-7440-239-15. Check that the punched tape reader performs in a normal manner. Check that the TIG NEXT NUMBER indicators do not change the count displayed.

## d. Back-to-Back Checkout Procedure, TIG.

(1) Insure the common control unit PC card A1A30 has been replaced with the new PC card (item 29,table 4-4].
(2) Failure to install the new PC card in the CCU A1A30 location will cause the CCU to hang up during back-to-back operation. Theory of operation and schematic diagrams of the CCU PC card A1A30 (part No. SM-E-546543) are provided in TM 11-7440-214-15.
(3) Perform initial turn-on procedures on the CCU as outlined in paragraph 3-2p, TM 11-7440-239-15.
(4) As determined by the particular terminal configuration, perform initial turn-on procedures on the paper tape punch (para 3-2g or 3-2i) that will be used as the output and receive monitor device for the paper tape reader being checked.
(5) The tests below assume that the output and monitor devices are ready for operation at all times. Unless specifically directed otherwise, keep the output devices adequately supplied with blank tape and paper.
(6) Before starting any test, read the entire test to become familiar with the procedure to be followed and the expected results.
(7) Preliminary test setup.
(a) Check that all ASSIGNED indicators on the CCU control panel are not illuminated. If any indicator is on, press the switch once to turn it off.
(b) Load the applicable output and monitor device with blank tape or paper and press the START switch on the devices. The START switches should light green and the NOT ASSIGNED indicators should light amber.
(c) Open the maintenance panel cover on the CCU and place the CCU TEST MODE SELECT switch in the I/O position. Press the MASTER RESET switch.
(d) At the CCU, press the SEND DEVICE ASSIGNED switch for the paper tape reader/TIG to be checked. Also press the appropriate RECEIVE DEVICE and RECEIVE MONITOR ASSIGNED switches. As each switch is pressed, it should light white. In addition, the NOT ASSIGNED indicator on the associated device should go out. The RECEIVE DEVICE and RECEIVE MONITOR READY indicators should light green.
(e) Press the CCU SEND DEVICE CANCEL switch. The switch should light momentarily
tarily, then the RECEIVE DEVICE RM indicator should go out,
(f) Perform the initial turn-on procedures for the punched tape reader/TIG to be checked as outlined in paragraph 3-2d, TM 11-7440-239-15.
(g) Insure the TIG ON-LINE/OFFLINE SWITCH in the ON-LINE position. Check that the TIG ON indicator is illuminated white.
(h) Set the TIG manual update thumb- wheel switches to 099 and then press the TIG LOAD switch. Check that the TIG NEXT NUM- BER indicators display 099.
(i) Prepare a paper tape test message consisting of approximately 100 characters. Use either ASCII or ITA \#2 code depending upon normal terminal operation. This message should have a line feed and carriage return after about 100 characters and an end-of-message sequence at the end of the message. Label this "Test tape A." It is recommended that two ends of this test tape be spliced to form a loop.
(j) Prepare a paper tape test message consisting of approximately 50 characters. Use either ASCII or ITA \#2 codes depending upon normal terminal operation. Do not use an end- ofmessage sequence and do not form this test tape into a loop. Label this "Test Tape B."
(k) Insure that the ASCII/ITA \#2 switches in both the punched tape reader and in the paper tape punch are set to the proper position for the tape message coding used. Also insure the proper code wheel is installed on the printer interpreter.
(I) Place the punched tape reader in low speed operation by pressing the HIGH SPEED/ LOW SPEED switch until the LOW SPEED indicator is illuminated.
(8) Message transfer test.
(a) Load test tape A into the punched tape reader leaving blank leader space before the first character of the message. Press the punched tape reader START switch and allow one message to be read.
(b) Check that the SEND DEVICE SELECT indicator on the CCU turns white and the punched tape reader START indicator turns white after the tape has advanced to the first character of the message.
(c) Observe that the TIG NEXT NUMBER indicator increments by one to read 100 at the same time that the punched tape reader START indicator illuminates white.
(d) The punched tape reader should then read the entire message and the receive output and monitor devices should start processing the message.
(e) When the last character of the message is read, the punched tape reader START indicator should turn green and the CCU SEND DEVICE SELECT indicator should go out. If using a tape loop for test tape A, manually stop the punched tape reader at this point. If tape is not looped, allow the tape to advance to the end of tape at which time the reader will automatically stop.
(f) Check that the paper tape punch and/ or the page printer copy the message correctly. The message copied by the receive devices should be identical to the message on test tape A except that the transmission identification (TI) sequence should be added to the beginning of the message. The complete TI sequence consists of the sixteen characters identified in paragraph 3-84. However, strapping performed in compliance with paragraph 4772d may shorten the sequence to 15,14 , or 13 characters. Also note that on the page printer copy, SI, SO, CR, LF, and NUL characters are machine functions and will not be printed.
(g) Check that the TI sequence positions 5, 6, and 7 reflect the proper channel designator for terminal identification.
(h) Check that the TI sequence positions 8, 9, and 10 reflect the proper message sequence number (in this case 099).
(9) Message sequence test.
(a) Load test tape A into the punched tape reader.
(b) Set the TIG manual update thumbwheel switches to 000 and press the TIG LOAD switch. NEXT NUMBER indicators should reflect 000.
(c) Press the punched tape reader START switch and read a minimum of 20 messages. If test tape A is not spliced into a loop, this will require reloading and restarting the tape reader each time an "out of tape" condition occurs.
(d) Check the copy from the output devices to insure that each of the messages is preceded by the TI sequence.
(e) Observe that the NEXT NUMBER indicators on the TIG increment by one at the beginning of each message. Count will sequence from 000 to 020.
(f) Check the copy from the output devices to insure the message sequence portion of
the TI increments by one on each message from 000 to 020.
(g) Load each of the following message sequence numbers into the counter and then process two messages. Insure the NEXT NUMBER display and the receive device copy properly reflect the counting of the message sequence counter.

## NOTE

Tape reader must be selected to enable loading the message sequence counter.

| Load counter to- | Sequence number reflected <br> in next 2 messages |
| :---: | :---: |
| 029 | $029-030$ |
| 039 | $039-040$ |
| 049 | $049-050$ |
| 059 | $059-060$ |
| 069 | $069-070$ |
| 079 | $079-080$ |
| 099 | $089-090$ |
| 199 | $099-100$ |
| 299 | $199-200$ |
| 499 | $299-300$ |
| 599 | $399-400$ |
| 699 | $499-500$ |
| 799 | $599-600$ |
| 999 | $699-700$ |

(10) Send alarm/cancel test.
(a) Record the count in the TIG NEXT NUMBER indicators.
(b) Load test tape B in the punched tape reader and start message transmission by pressing the tape reader START switch.
(c) Check that the punched tape reader STOP, TAPE OUT, and CANCEL indicators are illuminated red when the punched tape reader runs out of tape.
(d) Check that the TIG NEXT NUMBER indicator has been incremented by one.
(e) Load test tape A and restart the punched tape reader and allow message to be completely processed. Check the copy from the paper tape punch and/or page printer to insure the retransmitted message begins with the correct TI sequence.
(11) Sequence counter load inhibit test.
(a) Load test tape A and restart the punched tape reader.
(b) Immediately after the punched tape reader starts to process the paper tape message, press the SEND DEVICE EOB STOP switch on the
common control unit. When the punched tape reader stops operation, insure the punched tape reader START indicator is still illuminated white.
(c) Observe the count displayed in the TIG NEXT NUMBER indicator display.
(d) Set the TIG manual update thumbwheel switches to 123 and then press the TIG LOAD switch. Insure the TIG NEXT NUMBER display indicators do not change from the count observed in (c) above.
(e) At the common control unit, press the SEND CHANNEL EOB STOP switch and allow the message to be completed.
(12) Pilot header operation test.
(a) Record the count indicated in the TIG NEXT NUMBER display.
(b) Load test tape B into the punched tape reader and press the PILOT HEADER switch. The test should be fed through the punched tape reader.
(c) At the end of the tape, the punched tape reader should stop with the TAPE OUT indicator illuminated. The audible alarm should not sound and the CANCEL indicator should be out. The TIG NEXT NUMBER display should have been incremented by one.
(d) Load test tape A into the punched tape reader and press the START switch. The test tape should be fed through the punched reader. The count indicated in the TIG NEXT NUMBER display should not increment.
(e) Check that the message received at the paper tape punch and/or page printer contains the TI sequence, followed by the test tape $B$ and then by test tape A.
e. Terminal Back-to-back Test (TIG).
(1) Insure the TIG ON-LINE/OFF-LINE switch is in the ON-LINE position.
(2) Perform terminal back-to-back tests using the paper tape channel in accordance with procedures outlined in paragraph 2-5c, TM 117440-23915.
(3) Check received copy to insure proper TI sequence precedes each message.
f. On-Line Test (TIG).
(1) Insure the TIG ON-LINE/OFF-LINE switch is in the ON-LINE position.
(2) Perform those on-line tests that pertain to paper tape channel devices as outlined in paragraph 3-6 TM 11-7440-239-15.
(3) Check that the TIG NEXT NUMBER indicator increments by one for each message transmitted.

## Section IX. DISASSEMBLY AND REASSEMBLY OF TIG ASSEMBLY A7

## 4-74. Disassembly and Reassembly of TIG Chassis

a. Disassembly. Disassemble the TIG chassis 6 or 7, fig. 447 ) in the order of the index lumbers in figure 4-48. Access to component parts of the TIG chassis is gained either by turning knurled latch (31) counterclockwise approximately one turn and then pulling hinged front panel assembly (19) open, or by removing the four screws (1) to remove the access cover plate (2).

CAUTION
To insure latch (31, fig. P48) properly secures front panel assembly (19), always turn knurled knob on latch one to two turns counterclockwise before closing panel assembly. Then, close the panel and secure by turning knurled knob on the latch in a clockwise direction until tight.
b. Reassembly. Reassemble the TIG chassis in the reverse order of a above.


| 1 | Screw, flathead, No. 4-40, \% in. |
| ---: | :--- |
|  | long |
| 2 | Access cover plate |
| 3 | Cable strap |
| 4 | TIG cable assembly |
| 5 | Cable tie mounting device |
| 6 | Terminal lug |
| 7 | Terminal lug |
| 8 | Nut, hex., self-locking, No. 4-40 |
| 9 | Washer, flat, No. 4 |
| 10 | Cable clamp |
| 11 | Cable strap |
| 12 | Identification plate |
| 13 | Toggle switch (S1) |
| 14 | Toggle assembly (S3) |
| 15 | Light indicator (DS1) long |
| 16 | Lamp, No. 382 |
| 17 | Nut, hex, self-locking, No. 4-40 |
| 18 | Washer, flat, No. 4 |
| 19 | Front panel assembly long |
| 20 | Flexible cable |
| 21 | Nut, hex, self-locking, No. 2-56 |

22 Washer flat, No. 2
23 Screw, fathead, No. 2-56, 7/16 in. long
24 Switch assembly (S2)
25 Switch module (S2U, S2T, S2H)
26. Screw, panhead, No. 4-40, V in.
long
27 Lockwasher, No. 4
28 Washer, flat, No. 4
29 Standoff, No. 4-40, $1 / 4 \mathrm{in}$. Long
30 PC card A7A1 (No. 12-890082)
31 Latch
32 Nut, hex, self-locking, No. 4-40
33 Washer, flat, No. 4
34 Screw, panhead, No. 4-40, \% in.
52 Identification plate
35 Terminal board (TB1)
36 Marker strip
37 Screw, flathead, No. 4-40, $1 / 4 \mathrm{in}$.
56 Light filter lens
38 Nut, hex, self-locking, No. 440
39 Washer, flat, No. 4

40 Screw, flathead, No. 4-40, \% in.
long
41 Hinge
42 Spacer
43. Chassis to frame adapter, side 44 Strike catch
45 Chassis to frame adapter, side
46 Rubber grommet
47 Screw, flathead, No. 4-40, in. long
48 Screw, panhead, No. 4-40, V in. long
49 Washer, flat, No. 4
50 Chassis to frame adapter, bottom
51 Drive screw
53 Plastic grommet
54 Chassis assembly
55 Chassis
57 Blank front panel
58 Front panel mounting frame

Figure 4-48. Transmission identification generator assembly (AT), component location diagram.

## 4-75. Removal and Replacement of Integrated Circuit Modules on PC Card A7A1

a. Removal. All integrated circuits modules (Z1 through Z9 fig. 5-25) are removable from plug-in type sockets on the TIG assembly PC card A1 (30, fig. 4-48).
(1) Open the TIG front panel assembly (19, fig P48) to gain access to the PC card mounted on the rear side of the front panel.
(2) Observe the position of the integrated circuit module in its respective socket prior to removal.
(3) Remove the integrated circuit module by prying gently on both ends to pull module straight out of the socket to prevent bending of the module terminal pins.
b. Replacement. To replace a integrated circuit module, reverse the procedure outlined in a above taking care that all terminals are started into the socket before pressing the module into place.

## CAUTION

Three of the plug-in sockets (XZ4, XZ5, and XZ6, fig. 5-25) have more terminals than are on the integrated circuit modules which are plugged into these positions. Thus, it is important to insure that terminal 1 of the integrated circuit module is inserted into terminal 1 of the
respective socket. Terminal 1 of the socket is identified by a dot on the PC card. Refer to figure 5-1.2 to identify terminal 1 of the integrated circuit modules.

4-76. Removal and Replacement of Indicator Display Modules DS2U, DS2T, and DS2H
a. Removal.
(1) Open the TIG front panel assembly (19, fig. 4-48) to gain access to the PC card mounted on the rear side of the front panel.
(2) Remove the self-locking nut and washer ( 8 and 9 ) securing cable clamp (10).
(3) Remove the four screws, washers, and lockwashers (26, 27, and 28) holding the PC card Al (30) to the front panel. Do not unsolder either the flexible cable (20) or the TIG cable assembly (4) from the PC card.
(4) Twist the PC card to gain access to the front side and remove the defective display module (DS2U, DS2T, or DS2H. fig. 5-25) from the socket.
b. Replacement To replace the display module, reverse the procedure outlined in a above. Insure the notch identifying pin 1 of the display module (B, fig. 5-1.2) is on the bottom when the PC card has been properly positioned.

## Section X. INSTALLATION OF DRIVE MOTOR ON-OFF SWITCH FOR PUNCHED TAPE READERS EQUIPPED WITH TIG

## 4-77. General

a. Scope. This section contains the procedure for installing a drive motor on-off switch on punched tape readers equipped with Transmission Identification Generator (TIG) Kit MK-1583/ G. Included are listings of tools and parts required to implement this modification.
b. Purpose. This modification provides a method of turning off the tape reader drive motor to reduce mechanical wear when the tape reader is not in use, without the resetting of the TIG channel number display and channel number generator to 000 , as would be the case if the unit were powered down in the normal manner [para 2-7) and then powered up again when needed.
c. Application. This modification applies only to those punched tape readers (RP-154(P)/G) in which the TIG Kit MK-1583/G has been installed.

## 4-78. Materials and Tools Required

## a. Materials Required.

(1) Switch, toggle, SPST (FSN 5930-655-
1514).
(2) Wire, stranded, \#16 AWG (8 in. Ig,
black).
(3) Solder, lead-tin alloy (60/40), rosin core.
b. Tools Required.
(1) Electric drill (chuck size to accommodate $15 / 32 \mathrm{in}$. bit).
(2) Drill bit, $15 / 32$ inch.
(3) Drill bit, No. 31.
(4) Center punch.
(5) Hammer.
(6) Soldering iron.

## 4-79. Installation Procedure

a. Preliminary Procedure.
(1) Remove ac input to tape reader by operating circuit breaker on main panel box to OFF.

## NOTE

In dual tape readers, determine the location in which the TIG is installed and modify the associated power supply. Power supplies PS1 and PS2 are associated with TIG locations A7 and A8, respectively. If the unit contains
a dual TIG, modify both power supplies.
(2) Remove applicable power supply (fig. 13). Refer paragraph 4-25 for power supply removable procedure.
(3) Remove fuse cover plate (24, fig. 410) from power supply.
b. Drilling.
(1) On power supply front panel, locate and mark the centers of the two holes identified as A and $B$ in figure 4-49
(2) Using a center punch and hammer, center-punch the two marked holes, leaving a good indentation in the panel.

## CAUTION

Before drilling, place a block of wood or piece of metal in back of the front panel where the drill bit will come through. This is necessary to prevent damage to wiring or components. Be sure to remove all metal chips and burrs when drilling is completed.
(3) Drill the two holes using a No. 31 bit. (A $1 / 8$ inch bit will suffice if a No. 31 is not available.)
(4) Using the upper hole drilled in (3) above as a pilot, drill a 15/32 inch hole at location A. This will be the mounting hole for the switch. The smaller (lower) hole at B is for the switch lock ring.
c. Switch Installation.
(1) Disconnect yellow and blue wire from back of 120 VAC 10A DRIVE MOT fuseholder XF8 (fig. 4-49). Remove wire from harness to a length that will allow extension of wire to the new switch location. Allow some slack.
(2) Connect the yellow/blue wire disconnected from XF8 to upper terminal (side opposite keyway ) of switch to be installed (See para 478a(1).)

NOTE
Switch is equipped with screw-lug terminals, requiring appropriate terminal lugs on the connecting wires. The switch terminals can be converted to solder-lug.
terminals by removal of screws and lockwashers from the terminals.
(3) Connect an 8 -inch length of wire para 4-78a(2)) to lower terminal of toggle switch being installed.
(4) Install switch in hole A (fig. 4-49) with keyway down. Tighten securely, with lock ring tab in hole B.
(5) Solder other end of wire installed in (3) above to fuseholder XF8 terminal from which the yellow/blue wire was disconnected in (1) above.
(6) Identify new switch as DRIVE MOT ON on power supply front panel.
(7) Replace fuse cover plate (24 fig. 4-10 removed in a(3) above.
(8) Replace power supply into unit, replacing harness into clamp on back of power supply. Tighten clamp and replace nylon clamp on harness on bottom of equipment cabinet. Check operation.


Figure 4-49. Drive motor switch installation, drilling detail.

## CHAPTER 5

## PRINTED CIRCUIT CARD MAINTENANCE

INSTRUCTIONS

## Section I. GENERAL

## 5-1. Scope of PC Card Maintenance

a. This chapter includes instructions for performing corrective maintenance procedures on PC cards. Isolation of a malfunction in the punched tape reader to a PC card is given in chapter 4. The instructions in chapter 5 are used to isolate the malfunction to a defective part in the PC card and to replace the defective part.
b. PC card maintenance includes:
(1) Testing a suspected PC card.
(2) Troubleshooting using manual techniques.
(3) Replacement of defective parts.

## 5-2. Tools and Test Equipment Required

The tools and test equipment required for performing PC card maintenance are listed in appendix C.

## Section II. TROUBLESHOOTING PRINTED CIRCUIT CARDS

## 5-3. Testing Procedure

If a PC card is suspected of being defective, install it in a punched tape reader which is known to be otherwise operable. Then operate the punched tape reader with a CCU and a page printer to check if each possible type of character can be read (fig. 3-5). If all characters are correctly read and the controls and indicators on the control panel operate normally, the PC card being checked is considered good. If a malfunction occurs, locate and correct the fault as described in paragraphs 54 through 5-10.

## 5-4. General Troubleshooting Procedure

The first step in servicing a defective PC card is to perform a visual inspection. If this does not help in localizing the fault, signal tracing and signal substitution techniques are required.

## 5-5. Visual Inspection

Carefully inspect the PC card for evidence of overheating. Check for corrosion, loose connections, or broken components.

## 5-6. Signal Tracing

a. Place the PC card on an extender board and, with power off, install it in an otherwise operable punched tape reader. Operate the punched tape reader to simulate the condition under which the malfunction was observed, then use standard signal tracing techniques to isolate the defective part. A thorough knowledge of the operation of the punched tape reader circuits as given in chapter 3 is required to effectively use signal tracing techniques. Use the local test mode of the punched tape reader (LOCAL TEST switch-indicator A3Z9) to obtain repeating waveforms as successive characters are read. Use the single feed mode (SINGLE FEED switch-indicator A3Z6) to check one character at a time.
b. The voltages and waveforms at most test points may be observed with the oscilloscope. In general, signals at inputs and outputs of integrated circuit logic element modules switch between 3.3 and 4.5 volts dc (high) and between 0 and 0.6 volt dc (low). The technician should determine whether the voltage at a specific terminal is high
or low at any time by studying the operating conditions at that time. For voltages at inputs and outputs of discrete component logic circuits, refer to paragraph 3-22
c. For the location of parts on PC cards, refer to figures 5-2 |through 5-17. For the location of terminals on integrated circuit logic element modules, see figure 51. This figure applies to all types of integrated circuit logic elements.
d. Each lamp driver microcircuit module contains three independent lamp driver circuits. Figure 5-1.1 shows the location and numbering of terminals on the microcircuit module.
e. On those punched tape readers that have been converted by the addition of a transmission identification generator kit MK-1583/G, refer to figures 5-24|and 5-25 for location of parts on PC cards. For location of terminals on integrated circuit logic element modules on these PC cards, se figure 5-12.

## 5-7. Signal Substitution

Do not use signal substitution methods of troubleshooting the logic circuits in logic assembly. A-1. Connecting a ground at any point in the logic circuit to make operation predictable may cause circuit damage. Connecting a high level ( +4.5 volts) will not change the effect of a low level (ground) already existing at a point because of circuit operation.


Figure 5-1. Location of terminal on integrated circuit modules.

| TERMINAL | FUNCTION | TERMINAL | FUNCTION |
| :---: | :---: | :---: | :---: |
| 1 | OUTPUT | 6 | INPUT 3 |
| 2 | INPUT 1 | 7 | +12 VOLTS DC |
| 3 | OUTPUT 2 | 8 | -2 VOLTS DC |
| 4 | INPUT 2 | 9 | LAMP TEST |
| 5 | OUTPUT 3 | 10 | GROUND |



Figure 5-1.1. Location of terminals on microcircuit lamp driver modules

## Section III. REPAIR

## 5-8. General Parts Replacement Techniques

Most of the parts on a PC card can be replaced easily without special procedures. For PC card soldering techniques, refer to TB SIG 222 (Army), TO 00-25-234 (Air Force) or NW 0015PA-1 (Navy) (app. A). When replacing integrated circuit logic elements, it is important to unsolder only one terminal at a time, using a solder
syringe to remove the solder before unsoldering the next terminal.

## 5-9. Parts Location.

The location of all replaceable parts on the PC cards of the punched tape reader is shown in [figures 5-2 through 5-14.
terminal 6: +VC terminal 1: ground

type module
No
A

.775

terminal 14: $+V_{C c}$ terminal 7: ground

## 


PAR GEN - 74180 CONTROL - 74H87

D



5678


4321 bottom view type module display-I

B

| 7 |
| :---: |
| .250 |
| + |

type module
isolator MCD2


## E

TM 7440-219-15-137

Figure 5-1.2. Location of terminals on TIG integrated circuit modules.

Change 4-2.1

## Section IV. PRINTED CIRCUIT CARD TEST DATA CHARTS

## 5-10. Test Data Charts

a. The test data charts contained in this section may be used when troubleshooting printed circuit cards to determine the type of signal which should be present under certain conditions. This should prove as an aid in localizing a malfunction to a particular circuit on the suspected defective card.
b. For all cards installed in logic assembly AI, ground is available on pin 1 or $A$ of the printed circuit card connector. Pin 2 or B of each PC card connector supplies +4.5 volts to the printed circuit cards. By using a short lead terminated at both ends with alligator clips, these pins can be used as a source of ground ( O volt) or active (+4.5 volts) signals for troubleshooting the printed circuit cards.
c. Test data charts are arranged to show the point of test (Test point column) to which the meter, oscilloscope, or other test equipment is connected; the conditions under which the measurement should be made (Test conditions column); and the results which should be obtained if the circuit being tested is good (normal indication column). It should be noted that the Normal indication column gives the expected results for the specified test conditions, and not necessarily the results for normally operating equipment.
d. Unless otherwise specified, all test data in the charts assume the printed circuit board connected to an otherwise operable equipment, with the equipment operating as part of a terminal configuration.

## 5-11. PC Card A1 (A65209-001) Test Data Chart

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| XA1-5 or XA1-6 | PC card A14 removed from logic assembly A1 (fig. 4-8), power on, and- <br> a. +4.5 volts dc applied to input (XA1-D) <br> b. Ground applied to input (XA1-D) | a. -48 volts de <br> b. 0 volt dc |
| XA1-14 | Initial power-on | +4.5 volts de pulse <br> 330 ms wide with slow decay |
| XA1-T | Any power-on condition | 0 to +4.5 volt pulses at a $9.6 \mathrm{kHz} \pm 96$ Hz rate |

## 5-12. PC Card A3 (SM546659-001) Test Data Chart

figs. 5-14 and 8-8)

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| Typical lamp driver output (XA3-U). | PC card A15 removed from logic assembly A1 (fig. 4-8), power on, and- <br> a. LAMP TEST switch A3Z4 pressed <br> b. +4.5 volts dc applied to input (XA3-17) <br> c. Ground applied to input (XA3-17) | a. 0 volt dc <br> b. 0 volt dc <br> c. 15 volts ac |

## 5-13. PC Card A4 (A65215-001) Test Data Chart

> (jigs. 5-8 land 8-9)

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| Typical XMTR-1A output (XA4-14). | PC card A16 removed from logic assembly A1 (fig. 4-8), power on, and- <br> a. +4.5 volts de applied to input (XA4-16) <br> b. Ground applied to input (XA4-16) | a. 0 volt de <br> b. Open circuit $(+6.2$ volts may be reflected from receiver in CCU) |
| Typical RCVR-1A or RCVR-1R output (XA4-8). | Plug P1 removed from logic assembly A1 (fig. 4-8), power on, and- <br> a. Ground applied to input (XA4-9) <br> b. Open circuit applied to input (XA4-9) | a. +4.5 volts dc <br> b. 0 volt dc |


| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| XMTR-1R output (XA4-21). | PC card A16 removed from logic assembly A1 (fig. 4-8), power on, and- <br> a. Ground applied to both inputs (XA4-22) and (XA423). <br> b. Ground applied to input (XA4-22) and +4.5 volts dc applied to input (XA4-23). <br> c. +45 volts dc applied to both inputs (XA4-22) and XA4-23). | a. Open circuit ( +6.2 volts may be re flected from associated received in CCU) <br> b. Open circuit ( +6.2 volts may be reflected from associated receiver in CCU) <br> c. 0 volt dc |
| RCVR-1C output (XA4-D). | Plug P1 removed from logic assembly A1 (fig. 4-8), power on, and- <br> a. +6.2 volts de applied to input (XA4-E) <br> b. -6.2 volts dc applied to input (XA4-E) | a. +4.5 volts dc <br> b. 0 volt dc |

5-14. PC Card A5 (A65205-001) Test Data Chart
Fiias 5-6land 8-10)

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| Typical XMTR-2 output (XA5-U). | PC cards A4 and A6 removed from logic assembly A1 (fig. 4-8). power on, and- <br> a. +4.5 volts dc applied to gate input (XA5-10), then- <br> (1) +4.5 volts dc applied to input (XA5-W) <br> (2) Ground applied to input (XA5-W) <br> b. Ground applied to gate input (XA5-10) . then- <br> (1) +45 volts dc applied to input (XA5-W) <br> (2) Ground applied to input (XA5-W) | a. Output enabled <br> (1) +6.2 volts dc <br> (2) -62 volts dc <br> b. Output inhihited <br> (1) -6.2 volts de <br> (2) -6.2 volts dc |

## 5-15. PC Card A6 (A65421-001) Test Data Chart

tigs. 5-9 land 8-11)

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| XA6-19 | Power on, ASCII mode, with first character of TEST TAPE A-2 (para 5-11) in the read head. SINGLE FEED switch A3Z6 pressed 78 times observing the following test points at indicated number of single feed operations: <br> a. (Space) steps 3 and 37 | a. +45 volts dc; other steps show 0 volt dc |
| XA6-V | b. (Bell) step 4 | b. +4.5 volts dc ; other steps show 0 volt de |
| XA6-12 | c. (Shift Out) step 5 | c. +4.5 volts dc ; other steps show 0 volt de |
| XA6-C | d. (Delete) step 6 | d. +4.5 volts dc; other steps show 0 volt de |
| XA6-S | e. (Shift In) step 7 | e. +4.5 volts dc ; other steps show 0 volt dc |
| XA6-13 | f. (Null) step 8 | $f$. +4.5 volts dc ; other steps show 0 volt dc |
| XA6-8 | g. (Device Control 4) step 9 | g. +4.5 volts dc; other steps show 0 volt dc |
| XA6-J | h. (End of Medium) step 10 | h. +4.5 volts dc; other steps show 0 volt de |
| XA6-20 | i. (N) step 24 | i. +4.5 volts dc; other steps show 0 volt dc |
| XA6-3 | j. (@-Commercial At) step 48 | $j$. +4.5 volts dc; other steps show 0 volt dc |


| Test noint | Test condition | Normal indication |
| :---: | :---: | :---: |
| XA6-U | k. (Carriage Return) step 75 | $k .+4.5$ volts dc ; other steps show 0 volt de |
| XA6-11 | 1. (Line Fred) steps 76 and 77 | l. +45 volts de; other steps show 0 volt dc |
| XA6-14 | m. (IDC) steps $3,4,5,6,7,8,37,75,76$, and 77 | $m .+4.5$ volts dc; other steps show volt de |
| XA6-F | 21. (CB) All steps | n. 0 volt dc level |
| X $\mathrm{A}_{6-9}$ | o. (INC) All steps | o. 0 volt dc level |

5-16. PC Card A7 (A65425-001 Test Data Chart
Figs. 5-10 and 8-12)

| Test noint | Test condition | Normal indication |
| :---: | :---: | :---: |
| $\begin{gathered} \mathrm{A} 7-23 \\ -\mathrm{Y} \\ -\mathrm{N} \\ -\mathrm{P} \\ -\mathrm{S} \\ -\mathrm{U} \\ -\mathrm{R} \\ -16 \end{gathered}$ | Power on, ASCII mode with test tape A-1 loaded. LOCAL TEST switch A3Z9 pressed. <br> a. Character U loaded <br> b. Character * loaded | a. Output pins indicate $+4.5,0,+4.5$, $0,+4.5$ volts, and 0 volt dc , respectively. <br> b. Output pins indicate $0,+4.5,0,4.5$, $0,4.5,0$, and 4.5 volts dc , respectively. |

5-17. PC Card A8 (A53418-001) Test Data Chart
fiigs 5-2]and 8-13)

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| Typical row and COL decode gate Z15B (XA8-8). | Power on, ITA \#2 mode with test tape B-1 loaded. LOCAL TEST switch A3Z9 pressed. | Train of +4.5 to 0 -volt negative pulses |
| X ${ }^{\text {8 } 8-M ~}$ | Power on, ITA \#2 mode with test tape B-1 loaded. LOCAL TEST switch A3Z9 pressed. | One 0 - to +4.5 -volt positive pulse per line |
| XA8-11 | Power on, ITA \#2 mode with test tape B-1 loaded. LOCAL TEST switch A3Z9 pressed. | Two $0-$ to +4.5 -volt positive pulses per line |
| ZA8-16 | Power on, ITA \#2 mode with test tape B-1 loaded. LOCAL TEST switch A3Z9 pressed. | Two 0 - to +4.5 -volt positive pulses per line |
| XA8-S and -U | Power on, ITA \#2 mode with test tape B-1 loaded. LOCAL TEST switch A3Z9 pressed. | Complementary 0 - and +45 -volt de outputs changing several times per line |

## 5-18. PC Cards A9 and A11 (A53725-001) Test Data Chart

ffigs. 5-5, 8-4, and 8-16

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| Typical decode gate $\mathrm{Z} 4 \mathrm{~B}\left(\mathrm{CHU}^{\prime}\right)$ <br> (XA9-C). | Power on. ITA \#2 mode with test tape B-1 loaded. <br> a. MASTER RESET switch A1S1 pressed <br> b. LOCAL TEST switch A3Z9 pressed | a. 0 volt dc <br> b. One 0 - to +4.5 -volt positive pulse per line (character 32) |

## 5-19. PC Cards A10 and A12 (A53721-001) Test Data Chart

(figs. 5-4, 8-15, and 8-17)

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| Typical F line decode gate E-1 (Z11A and | Power on, ITA \#2 mrde with test tape B-1 loaded. a. MASTER RESET switch A1S1 depressed |  |


| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| X11B (XA10-H). | b. Depress LOCAL TEST switch A3Z9 <br> c. Further isolation can be provided by removing PC cards A9 and A11 from the logic assembly A1 (fig. 4-8), power on and- <br> (1) Ground apolied to innuts (XA10-F, XA10-E, XA10-L. and XA10-10). <br> (2) +4.5 volts dc applied to any one innut and ground annlied to the $0^{\text {ther }}$ inputs (XA10-F, XA10-E, XA10-L, and XA10-10). | b. Eight 0 - to +4.5 -volt de pulses per line <br> c. Observe the following: <br> (1) 0 volt de <br> (2) +4.5 volts dc |

## 5-20. PC Card A13 (A53434-001) Test Data Chart

(figs. 5-3land 8-18)

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| Typical ASCTI enc ${ }^{-}$de 1 thru 198 outputs (XA13-C). | Power on. ITA $\# 2$ mods with test tape R-2 Iraded. <br> a. Depress the MASTER RESET switch A1S1 <br> b. Depress LOCAL TEST switch A3Z9 | a. 0 volt de <br> b. Output will alternate between 0 and +4.5 volts dc as each 4th character is read |

5-21. PC Card A14 (A65433-001) Test Data Chart
[figs 5-12|and 8-12)

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| Typical binary counter flip-flop outputs (XA14-11). | Power on, ASCII or ITA \#2 mode and low-speed operation, single feed or lncal test will cause the binary counter to cycle one time for each character position on the paper tape. | 0 - and +4.5 -volt de pulses. (number of pulses generated depends on the binary value of the flip-flops being checked) |
| XA14-21 | Power on, any mode- <br> a. With the reador in high speed operation, depress the SINGLE FEED switch A3Z6. <br> b. With the reador in low spsed operation, depress the SINGLE FEED switch A3Z6. | a. 0 - to +4.5 -volt de positivo pulse 666 ms after pressing SINGLE FEED switch <br> b. 0 - to +4.5 -volt dc positive pulse 53.4 ms after pressing the SINGLE FEED switch |
| XA14-C | Power on, any mode and depress the SINGLE FEED switch, A3Z6. | Two 0- to +4.5 -volt de positive pulses $104 \mu$ sec wide |
| XA14-3 | Power on, any mode and depress the SINGLE FEED switch A3Z6. | 0 - to +4.5 -volt de positive pulses, 1872 $\mu \mathrm{sec}$ wide from count 1 to count 18 |
| XA14-4 | Power on, any mode and depress the SINGLE FEED switch A3Z6. | Eight 0- to +4.5 -volt dc positive pulse $208 \mu \mathrm{sec}$ wide |
| XA14-M | Power on, any mode and- <br> a. With the reader in high speed operation depress the SINGLE FEED switch A3Z6. <br> b. With the reader in low speod operation, depress the SINGLE FEED switch A3Z6. | a. 0 -volt dc level, however 20 ms noise spikes will appear <br> b. 0 - to +45 -volt dc level, after 6.6 ms. Signal should remain at $+4.5-$ volt de level until the end of the counter cycle ( 53.4 ms ) |

## 5-22. PC Card A15 (A65437-001) Test Data Chart

(figs. 5-13land 8-20)

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| XA15-21 | Power on. not assigned, and depress the MASTER RESET switch A1S1. | +4.5 -volts dc while switch is depressed, otherwise 0 -volt dc level |


| Teat point | Teat condition | Normal indication |
| :---: | :---: | :---: |
| XA15-Y | Power on, not assigned, with any test tape loaded with the leader in the read station, and- <br> a. Depress the MASTER RESET switch A1S1 <br> b. Depress the START switch A3Z7 | a. +4.5-volt dc level <br> b. +4.5- to 0 -volt dc transition when first data character enters read station |
| XA15-Z | Power on, not assigned and MASTER RESET switch A1S1 depressed. | +4.5 -volts dc while switch is depressed, otherwise 0 -volt dc level |
| XA15-V | Power on reset condition with PC cards A6 and A14 removed from the logic assembly A1 (fig. 4-8) and - <br> a. Ground applied to the inputs (XA15-X, XA15-W, and XA15-22). <br> b. Ground applied to inputs (XA15-2 and XA16-W) and +4.5 volts de applied to input (XA15-22). | a. $\mathbf{+ 4 . 5}$ volts dc <br> b. 0 -volt to +4.5 -volt dc positive pulse 104 $\mu \mathrm{sec}$ wide |
| XA15-3 | Power on with any test tape loaded and - <br> a. Depress the MASTER RESET switch A1S1 <br> b. Depress LOCAL TEST switch A3Z9 with the reader operating, the TIGHT TAPE switch on the reader mechanism manually activated. | a. +4.5 volts dc <br> b. 0 volt dc |
| XA15-J | Power on with any teat tape loaded and- <br> a. Depress the MASTER RESET switch A1S1 <br> b. Depress the LOCAL TEST awitch A3Z9 and a tape motion failure manually develops. | a. +4.5 volts dc <br> b. 0 volt dc |

5-23. PC Card A16 (A65429-001) Test Data Chart
figs. 5-11 and 8-21)

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| XA16-C. | Power on with any test tape loaded and- <br> a. Depress the MASTER RESET switch A1S1 <br> b. Depress START switch A3Z7 | a. +4.5 volts de <br> b. 0 volt dc |
| XA16-Y. | Power on with any test tape loaded and- <br> a. Depress the MASTER RESET switch A1S1 <br> b. Depress SINGLE FEED switch A3Z6 | a. 0 volt de <br> b. 0 -volt to +4.5 -volt dc positive pulse 3.5 ms wide |
| XA16-8 | Power on with any test tape loaded and- <br> a. Depress the MASTER RESET switch A1S1 <br> b. Depress START switch A3Z7 | a. 0 volt dc <br> b. +4.5 volts dc |
| XA16-9 | Power on with any test tape loaded and- <br> a. Depress the MASTER RESET switch A1S1 <br> b. Depress LOCAL TEST switch A3Z9 | a. +4.5 volts dc <br> b. 0 volt dc |
| XA16-15 | Power on with any test tape loaded and- <br> a. Depress the MASTER RESET switch A1SI <br> b. Depress the PILOT HEADER switch A3Z5 | a. 0 volt dc <br> b. +4.5 volts dc |
| XA16-21 | Power on, assigned and AUDIBLE RESET switch depressed. | $0-$ to +4.5 -volt dc positive pulse at least 500 $\mu \mathrm{sec}$ wide |

## CAUTION

When taking voltage measurements power supply PS1, sequence module A12 use insulated test connectors

## 5-24. Power Supply (PS1) Test Data Chart

(figs. 4-10, 8-4, and 86)

| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| $\begin{aligned} & \text { PS1TP2 to PS1TP1 } \\ & \text { (common). } \end{aligned}$ | Power on | +4.75 volts dc $\pm 1 \%$ |
| PS1TP3 to PS1TP1 | Power on | +12.0 volts dc $\pm 1 \%$ |
| PS1TP4 to PS1TP1 | Power on | -12.0 volts dc $\pm 1 \%$ |
| PSITP5 to PS1TP1 | Power on | -48.0 volts dc $\pm 1 \%$ |


| Test point | Test condition | Normal indication |
| :---: | :---: | :---: |
| PS1A12TP3 to PS1A12TP13. | Power on | -12.0 volts de $\pm 1 \%$ |
| PS1A12TP4 to PS1A12TP13. | Power on | +12.0 volts de $\pm 1 \%$ |
| PS1A12TP6 to PS1A12TP13. | Power on | +4.75 volts de $\pm 1 \%$ |
| PS1A12TP9 to PS1A12TP13. | Power on | -48.0 volts dc $\pm 1 \%$ |
| PS1A12TP11 to PS1A12TP13. | Power on | +15.0 volts dc $\pm 1 \%$ |



Figure 5-2. PC card No. A53418 (A8), component location diagram


Figure 5-3. PC card No. A53434 (A13), component location diagram.


Figure 5-4. PC card No. A63721 (A10, A12), component location diagram.


Figure 5-5. PC card No. A53725 (A9, A11), component location diagram


Figure 5-6. PC card no A65205 (A5), component location diagram.


Figure 5-7. PC card No. A65209 (A1), component location diagram.


Figure 5-8. PC card No. A65215 (A4),component location diagram.


Figure 5-8.1. PC card No. A65223 (A4), component location diagram
Change 2 5-8.2


Figure 5-8.2. PC card No. A65227 (A5), component location diagram


Figure 5-9. PC card No. A65421 (A6), component location diagram.


Figure 5-10. PC card No. A65425 (A7), component location diagram.

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(211)

25


Figure 5-11. PC card No. A65429 (A16), component location diagram.


Figure 5-12. PC card No. A65433 (A14), component location diagram.


Figure 5-13. PC card No. A65437 (A15), component location diagram.


Figure 5-14. PC card No. SM-E-546GG59 (A3), component location. diagram.


TM7440-219-15-80-1

Figure 5-15. Component board assembly (+4.75 VDC) (PSIAI), component location" diagram.


TM7440-219-15-89-1

Figure 5-16. Component board assembly ( $\pm 12$ VDC) (PS1A2), component location diagram.


TM7440-219-15-90-1

Figure 5-17. Component board assembly (-48 VDC) (PS1A3), component location diagram.


Figure 5-18. Power Supply heat sink assembly A4, component location diagram.


Figure 5-19. Power supply heat sink assembly A5, component location diagram.

CAVTION: When replacing semiconductor components of heat sink subassemblies A4, A5, or A6, clean mating surfaces of semiconductor and heat sink chassis and apply a light coat of Dow Corning DC 340 silicone grease to mating surfaces before mounting the semiconductor.


TM7440-215-15-104-1

Figure 5-20. Power supply heat sink assembly A6, component location diagram
Change 4 5-20


Figure 5-21. Power supply connector bracket assembly PSLU/4 and component board assembly PSIA15, component location diagram,

Change 7 5-21


Figure 5-22. Power supply .manual control card.


Figure 5-23. Power supply seque7Te module component board assembly PSIA12, component location diagram.

Change 4 5-23


Figure 5-24. TIG PC card No. 12-890081 (A1A2, A4A2), component location diagram,

ASSY 12-89001


TM 7440-299.

Figure 5-25. TIG assembly PC card No. 12-90082 (A7A1, A8A1), opponent location diagram.
Change 4 5-25/(5-26 blank)

## CHAPTER 6

## DEPOT MAINTENANCE

## Section I. DEPOT REPAIR

## 6-1. General

Complete rebuild of the punched tape reader may be accomplished by depot maintenance facilities, when authorized by appropriate authority. Rebuild action includes all repairs, rebuild, and replacement necessary to make this equipment equivalent to new material and suitable for return to the military supply system for reissue to using organizations.

## 6-2. Depot Repair

Depot repair includes all repair procedures described in chapters 4 and 5, in addition to the part fabrication and refinishing procedures possible with the metalworking and refinishing available at a depot.

## Section II. DEPOT OVERHAUL STANDARDS

## 6-3. Applicability of Depot Overhaul

## Standards

Reader, Punched Paper Tape RP-154 (P)/G (paper tape reader) must be tested thoroughly after repair to insure that it meets adequate performance requirements for return to stock and reissue. Use the tests described in this section to measure the performance of the repaired device. Equipment that is to be returned to stock should meet all of the performance standards given in this section. Depot overhaul standards also outline procedures for testing punched tape readers that have been modified by the addition of a Transmission Identification Generator Kit MK-1583/G.

## 6-4. Applicable References

a. Repair Standards.

Applicable procedures of the depots performing this test and the general

## Item Description

Frequency Counter (2 required)-- Beckman, Model 7350A, or equivalent accuracy of 1 part in 10' per week. Paper Tape Reader Test Set---- General Dynamics Electronics Division Model 48-200769 or equivalent. Timer, 1 minute ------------------- Standard, TF-4570.
Regulated Power Amplifier ------ CML Model N500A, or equivalent, with $0.5 \%$ c accuracy.
Plug-in Amplifier ------------------- AML Model SG13A, or equivalent, with 0.25', accuracy.
Test Cable -------------------------- Test cable terminated in 48-pin connector on one end and two fanning strips and
single No. 8 wire on other end. Cable is labled "Reader".
Test Tape Sample A ------------- ASCII code, 1-inch fully perforated tape, punched with each of the seventy-three
allowed combinations and interspersed with "Space" characters to take the place
of invalid codes in the ASCII sequence per table 6-1.This pattern will be re-
peated four times in succession and spliced in a loop.

## Item Description

Test Tape Sample B------- ASCII code, 1-inch fully perforated tape punched with all one-hundred and twentyeight possible combinations per table 6-2. This tape will be unspliced and index marked as shown in figure 6-1.
Test Tape Sample C------ ASCII code, 1 -inch fully perforated tape punched with the following sequences.(See fig.6-2.):
a. Fifty Nulls
h. Seven "idle" characters
c. Fifty Nulls
d. One hundred and twenty-eight characters including the seventythree allowed combinations as described for test tape sample A
e. Fifty N's
f. Fifty Nulls
g. Seven "idle" characters
h. Ten feet of Nulls

The "idle" characters consists of-

1. Null
2. Line Feed
3. Carriage Return
4. Shift-in
5. Shift-out
6. Delete
7. Space

Test Tape Sample D--- One-inch, fully perforated tape, punched with nulls, except for a single character "A" punched approximately midway between the ends of the tape. A printed character
" A " appears on the tape between sprocket holes at a distance of four and one-half character spacings ahead of the punched code "A".(See fig.6-2.) This tape is
unspliced.
Test Tape Sample E-------11/16-inch tape, chadless, punched with nulls, except for a single character "A" punched approximately midway between the ends of the tape. A printed character
" A " appears on the tape at a distance of six character spacings behind the punched code "A" (fig.6-2). This tape is unspliced.
Test Tape Sample F --------- ITA No 2 code. 1 -inch fully perforated tape punched to include each of the fiftyeight possible combinations repeated in succession four times in accordance with table 6-3 and spliced in a loop
Test Tape Sample G ------- Fully perforated 11/16-inch tape punched in the same manner as Test Tape F.
Test Tape Sample H ------- Fully perforated 7/'8-inch tape punched in the same manner as Test Tape F.
Test Tape Sample J.--- 1-inch tape punched in the same manner as Test Tape F, except that this tape is not spliced in a loop.
Test Tape Sample K--- 1-inch tape punched in the same manner as Test Tape F except that eight sprocket holes are torn in succession.
Test Tape Sample L.------ 11/16-inch tape, punched in the same manner as Test Tape F except tape will be chadless.
Test Tape Sample M------- ASCII code.1-inch fully perforated tape punched as indicated in table 6-4 The 100 -character pattern is to be repeated twice and the tape spliced into a loop.
Note Test Tape Sample $M$ is required only if a punched tape reader having a Transmission Identification Generator Kit MK-1583/G installed is to be tested.

Test Tape Sample P ------ Fully perforated, 1-inch tape, punched with alternate asterisk and UASCII code characters and spliced to form a loop.
TTG Simulator .------------ General Dynamics, Electro Dynamics Division model No.10-000231, or equivalent.
Note TIC, simulator is required only if a Transmission Identification Generator Kit MK-1.583/G is installed on the punched tape reader to be tested. In addition. the TIC, simulator Is not required if a dual TITG installation is to be tested that has an interconnecting cable installed between the two TIC assemblies.


NOTES

1. A dovele inoexing mark wil appear to the right of the INDEXING EDGE OF THE TAPE REAOER COVER FOR THE FIRST CHARACTER WHICH IS NOT AN "IOLE" CHARACTER.
2. A SINGLE indexing mark will appear to the right of the indexing edge of the tape reader cover for each invalio Character read.

Figure 6-1. Test tape sample B, index markings.
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TEST TAPE SAMPLE $C$,


TEST TAPE SAMPLE D,


TEST TAPE SAMPLE E,


Figure 6-2. Test tape sample $C, D$, and $E$.

Table 6-1. ASCII Test Pattern Character Sequence

| ASCII |  |  |  |  |  |  |  | Character |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |  |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NULL |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | BEL |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | LF |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | CR |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | SO |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | SI |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | DC4 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | EM |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | ! |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | " |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | \# |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | \$ |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | $\%$ |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | , |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | ) |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | * |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | + |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | , |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | - |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | . |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 2 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 3 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 4 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 5 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 6 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 7 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 8 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 9 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | , |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | ; |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | $<$ |



Table 6-1. ASCII Test Pattern Character Sequence-Continued

| ASCII |  |  |  |  |  |  |  | Character |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |  |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |


| ASCII |  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | Character |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | DEL |

Table 6-2. ASCII Binary Sequence for Test Tape B

| ASCII |  |  |  |  |  |  |  | Character |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |  |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SOH |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | STX |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | ETX |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | EOT |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | ENQ |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | ACK |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | BEL |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | BS |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | HT |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | LF |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | VT |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | FF |
| 1. | 0 | 1 | 1 | 0 | 0 | 0 | 1 | CR |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | SO |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | SI |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | DLE |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | DC1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | DC2 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | DC3 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | DC4 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | NAK |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | SYN |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | ETB |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | CAN |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | EM |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | SS |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | ESC |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | FS |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | GS |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | RS |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | US |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | ! |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | " |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | \# |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | \$ |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | $\%$ |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |  |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | $($ |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | ) |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | * |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | + |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |  |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | - |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | - |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 2 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 3 |


| ASCII |  |  |  |  |  |  |  | Character |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |  |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 4 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 5 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 6 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 7 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 8 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 9 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | : |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | ; |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | $<$ |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | $=$ |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | $>$ |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | ? |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |  |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | A |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | B |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | D |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | E |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | F |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | G |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | H |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | I |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | J |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | K |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | L |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | M |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | N |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | P |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | Q |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | R |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | S |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | T |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | U |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | V |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | W |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | X |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | $Y$ |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | Z |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | [ |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | $\sim$ |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | ] |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | $\wedge$ |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | - |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | @ |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | a |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | b |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | c |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | d |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | e |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | $f$ |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | g |

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Table 6-2. ASCII Binary Sequence for Test Tape B-Continued.

| ASCII |  |  |  |  |  |  |  | Character |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |  |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | h |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | i |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | j |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | k |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | m |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | n |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | p |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | q |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | r |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | s |


| ASCII |  |  |  |  |  |  |  | Character |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | 8 | 4 | $\checkmark$ | 6 | 7 | 8 |  |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | t |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | u |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | v |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | w |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | x |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | $y$ |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | $z$ |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | $\Sigma$ |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | - |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | \} |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | DEL |

Table 63. ITA No. 2 Test Pattern Character Sequence for Test Tapes F Through L

| ITA No. 2 |  |  |  |  | Character |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | 8 | 4 | 5 |  |
| 0 | 0 | 0 | 0 | 0 | BLANK |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 1 | 1 | 0 | 1 | 1 | FIGURES |
| 1 | 0 | 1 | 0 | 0 | BELL |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 1 | 0 | 0 | 0 | LINE FEED |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 0 | 1 | 0 | CARRIAGE RETURN |
| 1 | 1 | 0 | 1 | 1 | FIGURES |
| 1 | 1 | 1 | 1 | 1 | LETTERS |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 1 | 1 | 0 | 1 | 1 | FIGURES |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 1 | 0 | 1 | 1 | 0 | ! |
| 1 | 0 | 0 | 0 | 1 | " |
| 0 | 0 | 1 | 0 | 1 | \# |
| 1 | 0 | 0 | 1 | 0 | \$ |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 1 | 0 | 1 | 1 |  |
| 1 | 1 | 0 | 1 | 0 | , |
| 1 | 1 | 1 | 1 | 0 | ( |
| 0 | 1 | 0 | 0 | 1 | ) |


| ITA No. 2 |  |  |  |  | Character |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | 3 | 4 | 5 |  |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 1 | 0 |  |
| 1 | 1 | 0 | 0 | 0 | - |
| 0 | 0 | 1 | 1 | 1 | . |
| 1 | 0 | 1 | 1 | 1 | $/$ |
| 0 | 1 | 1 | 0 | 1 | ZERO |
| 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 2 |
| 1 | 0 | 0 | 0 | 0 | 3 |
| 0 | 1 | 0 | 1 | 0 | 4 |
| 0 | 0 | 0 | 0 | 1 | 5 |
| 1 | 0 | 1 | 0 | 1 | 6 |
| 1 | 1 | 1 | 0 | 0 | 7 |
| 0 | 1 | 1 | 0 | 0 | 8 |
| 0 | 0 | 0 | 1 | 1 | 9 |
| 0 | 1 | 1 | 1 | 0 | : |
| 0 | 1 | 1 | 1 | 1 | ; |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 0 | SPACE |
| 1 | 0 | 0 | 1 | 1 | ? |
| 1 | 1 | 1 | 1 | 1 | LETTERS |
| 1 | 1 | 0 | 0 | 0 | A |
| 1 | 0 | 0 | 1 | 1 | B |
| 0 | 1 | 1 | 1 | 0 | C |
| 1 | 0 | 0 | 1 | 0 | D |
| 1 | 0 | 0 | 0 | 0 | E |
| 1 | 0 | 1 | 1 | 0 | F |
| 0 | 1 | 0 | 1 | 1 | G |
| 0 | 0 | 1 | 0 | 1 | H |
| 0 | 1 | 1 | 0 | 0 | I |
| 1 | 1 | 0 | 1 | 0 | J |
| 1 | 1 | 1 | 1 | 0 | K |
| 0 | 1 | 0 | 0 | 1 | L |
| 0 | 0 | 1 | 1 | 1 | M |
| 0 | 0 | 1 | 1 | 0 | N |
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | $\mathbf{P}$ |
| 1 | 1 | 1 | 0 | 1 | Q |
| 0 | 1 | 0 | 1 | 0 | $\boldsymbol{R}$ |
| 1 | 0 | 1 | 0 | 0 | S |

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Table 6-3. ITA No. 2 Test Pattern Character Sequence for Test Tapes F Through L--Continued

| ITA No. 2 |  |  |  |  | Character | ITA No. 2 |  |  |  |  | Character |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | 3 | 4 | 5 |  | 1 | 2 | 3 | 4 | 5 |  |
| 0 | 0 | 0 | 0 | 1 | T | 1 | 1 | 0 | 1 | 0 | J |
| 1 | 1 | 1 | 0 | 0 | U | 1 | 1 | 1 | 1 | 0 | K |
| 0 | 1 | 1 | 1 | 1 | V | 0 | 1 | 0 | 0 | 1 | L |
| 1 | 1 | 0 | 0 | 1 | W | 0 | 0 | 1 | 1 | 1 | M |
| 1 | 0 | 1 | 1 | 1 | X | 0 | 0 | 1 | 1 | 0 | N |
| 1 | 0 | 1 | 0 | 1 | Y | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | Z | 0 | 1 | 1 | 0 | 1 | P |
| 0 | 0 | 1 | 0 | 0 | SPACE | 1 | 1 | 1 | 0 | 1 | Q |
| 0 | 0 | 1 | 0 | 0 | SPACE | 0 | 1 | 0 | 1 | 0 | R |
| 0 | 0 | 1 | 0 | 0 | SPACE | 1 | 0 | 1 | 0 | 0 | S |
| 0 | 0 | 1 | 0 | 0 | SPACE | 0 | 0 | 0 | 0 | 1 | T |
| 0 | 0 | 1 | 0 | 0 | SPACE | 1 | 1 | 1 | 0 | 0 | U |
| 0 | 0 | 1 | 0 | 0 | SPACE | 0 | 1 | 1 | 1 | 1 | V |
| 1 | 1 | 0 | 0 | 0 | A | 1 | 1 | 0 | 0 | 0 | W |
| 1 | 0 | 0 | 1 | 1 | B | 1 | 0 | 1 | 1 | 1 | X |
| 0 | 1 | 1 | 1 | 0 | C | 1 | 0 | 1 | 0 | 1 | Y |
| 1 | 0 | 0 | 1 | 0 | D | 1 | 0 | 0 | 0 | 1 | Z |
| 1 | 0 | 0 | 0 | 0 | E | 0 | 0 | 1 | 0 | 0 | SPACE |
| 1 | 0 | 1 | 1 | 0 | F | 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 1 | 0 | 1 | 1 | G | 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 0 | 1 | 0 | 1 | H | 0 | 0 | 1 | 0 | 0 | SPACE |
| 0 | 1 | 1 | 0 | 0 | I | 0 | 0 | 1 | 0 | 0 | SPACE |

Table 6-4. Tig Test Tape Sample M

| ASCII |  |  |  |  |  |  |  | Character |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |  |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | T |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | H |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | I |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | S |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | I |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | S |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | A |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | T |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | E |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | S |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | T |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | F |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | T |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | I |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | G |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | A |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | B |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | D |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | E |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | $F$ |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | G |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | H |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | I |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | J |


| ASCII |  |  |  |  |  |  |  | Character |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | 3 | 1 | 6 | 6 | 7 | 8 |  |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | K |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | L |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | M |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | N |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | P |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | Q |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | R |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | S |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | T |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | U |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | V |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | W |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | X |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | Y |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | Z |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 2 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 3 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 4 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 5 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 6 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 7 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 8 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 9 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | - |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | - |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | - |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | - |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |

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Table 6-4. Tig Test Tape Sample M-Continued.

| ASCII |  |  |  |  |  |  |  | Character |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |  |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SPACE |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | CR |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | CR |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | LF |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | LF |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | N |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | N |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | N |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | N |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | DEL |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | DEL |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | DEL |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | DEL |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | DEL |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | DEL |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | DEL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |


| ASCII |  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathbf{1}$ | $\mathbf{2}$ | $\mathbf{3}$ | $\mathbf{4}$ | $\mathbf{5}$ | $\mathbf{6}$ | $\mathbf{7}$ | $\mathbf{8}$ | Character |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NUL |

6-6. General Test Conditions and

## Requirements

Before the tests (bara 6-7) through 6-9) are made, the equipment shall meet the mechanical requirements specified in a below. The general test conditions of $b$ below shall be established. Paper tape reader test set must be modified as outlined in c below before testing transmission identification generator.
a. Mechanical Requirements.
(1) The paper tape reader should be assembled for 120 VAC, 60 Hertz operation, and should be adjusted to meet the requirements of baragraphs 4-47 through 4-66
(2) Reader mechanism should be lubricated per the procedure of paragraph 4-8 before starting the tests of this section.
b. Test Conditions.
(1) Unless otherwise specified, all tests will be performed under the following test conditions:
Temperature ------
Altitude - $\qquad$
Ambient, 150 C to $35^{\circ} \mathrm{C}$
Humidity $\qquad$
Normal ground
Room ambient up to $98 \% 0$
Power
120 VAC, 60 Hertz
(2) Connect the paper tape reader to the test equipment as shown ir figure 6-3.
(3) When the test procedure requires test tape samples to be loaded into the read head, the following procedure should be followed:
(a) Splice tape loops using a butt splice, and place the splice on the outside of the loop.

Place tape loops in the read head with the splice up.
(b) When it is desired to begin reading on a punched character, it is necessary to manually slew the tape to the desired starting character. To do this, the tape is placed in the read head and the cover is closed, the slewing lever is placed in the slewing position, and the tape is manually moved to the desired starting point. The slewing lever is then returned to its original position before starting the reader. This procedure is to be followed when loading the test tapes called for in the test procedure.
(c) ITA test tape samples F, G, $\mathrm{H}, \mathrm{K}$, and L are to be marked with and loaded at a START position to insure that the test set search operation locates the proper reference character. The START position is to be marked by a single line drawn across the tape adjacent to the LETTERS character in table 6-3 as shown in figure 6-4. The tape is then to be loaded and positioned in the read head such that the START index line is adjacent to the indexing edge of the tape cover.
c. Paper Tape Reader Test Set Modification. Modification of paper tape reader test set, general dynamics electro dynamic division model 48200769, is required to enable testing of punched tape reader units that have been modified with the addition of one or two Transmission Identification Generator Kits MK-1583/G. Perform the following on the paper tape reader test set to complete this modification:
(1) Add a wire from the test set terminal board TB3-20 (EM signal line) to a spare test


Figure 6-3. Test setup.


Figure 6-4. Placement of test tape start index line.
point on the test set front panel. Label the test point "EM." It is noted that some of paper tape reader test sets were not manufactured with
spare test points. In this case, it will be necessary to first mount a test point similar to the type used for other test points on the test set.

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(2) Connect a 1200 -ohm resistor (MIL type RC07GF122J) between the EM test point and +12 VDC.
(3) Connect a 1200 -ohm resistor (MIL type TC07GF122J) between the EM test point and ground.
d. Fabrication of TIG Simulator. In lieu of using TIG simulator, general dynamics, electro dynamic division model No. 10-000231, you may fabricate a TIG simulator in accordance with the following (electrical schematic of the circuit is illustrated in fig. 6-5):
(1) Obtain a small chassis and mount a switch (S1) on the chassis. The switch should be a momentary action, single-pole, doublethrow chassis switch with all contacts isolated from ground.
(2) Mount a test point (TP1) on the chassis. Recommend a type similar to those used in the paper tape reader test set.
(3) Obtain a Texas instrument type SN7474J integrated circuit module, FSN 59624701637 (type SN7474N may be substituted) and make the following connections to switch S1. Insure all terminals of the integrated circuit flipflop are isolated from the chassis.
(a) Connect the common contact of S1 to flip-flop Z1 terminal 7.
(b) Connect the normally-closed contact of switch S1 to flip-flop Z1 terminal 10.
(c) Connect the normally-open contact of switch S1 to flip-flop Z1 terminal 13.
(4) Obtain five wires, AWG No. 20, 3 to 4 feet long, to fabricate an interconnection cable. Label these wires and connect to the TIG simulator as follows:
(a) Wire No. 4-Connect to terminal 14 of the flip-flop Z1.
(b) Wire No. 5--Connect to test point TP1.
(c) Wire No. 6--Connect to switch S1 common terminal.
(d) Wire No. 7-Connect to terminal 14 of the flip-flop Z1.
(e) Wire No. 8-Connect to terminal 9 of the flip-flop Z1.
(5) Lace the wires in the cable and attach five terminal lugs, type MS25036-101 or equivalent, to the end of the cable. The wire numbers labeled in (4) above indicate the terminal numbers of the connections to the TIG terminal board TB1.


Figure 6-5. TIG simulator, schematic diagram.

## 6-7. Visual Tests

Disconnect power from the device. Check the general physical condition of the equipment as follows:
a. Exterior and Interior Surfaces. All surface finishes must be free from rust, scratches, or other damage. Surfaces must not be damaged.
b. Cables. The lead connections of all cables must be secure. All cable connectors must be undamaged and cables should not be cracked, frayed, or routed to place strain on the wires.
c. Hardware. All bolts and screws, such as slide mounting screws, panel mounting screws, motor mounting bolts, and mechanism mounting screws must be tight.
d. PC Cards. Check that all printed circuit cards in logic assembly Al are mounted securely in the proper connector (para 1-6].

6-8. Operational Tests-Fixed Voltage and Frequency
a. Preliminary Procedure.
(1) Set the switches and controls on the paper tape reader test set as follows:

115 VAC circuit breaker to OFF
CANCEL to OFF
SELECT to OFF
SPEED (rotary switch) to NORM
COMPARATOR INPUT to DATA IN
EOB 'EOM to OFF
ASSIGN 'NOT ASSIGN to NOT ASSIGN
COMPARATOR to ON
AUTO/MAN to AUTO
SE ,, RCH/TEST to SEARCH
ASCII/ITA 2 to ASCII
(1.1)Connect jumper wires
between strapping option standoff terminals on the punched tape reader PC card A2 as indicated in table 65 , TI Sequence 1 column.

Table 6-5. Strapping jumpers, PC Card A2

| Strapping option | Connect jumper wire from terminal | Connect jumper wire to terminal |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TI Sequence number 1 | TI Sequence number 2 | TI Sequence | TI Sequence |
| TI start postion. | $2^{\circ}$ | 0 | 1 | 0 | 1 |
|  | $2^{1}$ | 0 | 0 | 1 | 1 |
| First channel designation character. | 1A | 1 | 0 | 0 | 0 |
|  | 2 A | 0 | 1 | 1 | 1 |
|  | 3A | 0 | 1 | 1 | 1 |
|  | 4A | 0 | 1 | 1 | 1 |
|  | 5A | 0 | 1 | 1 | 1 |
|  | 6A | 0 | 1 | 1 | 1 |
|  | 7A | 1 | 0 | 0 | 0 |
| Second channel designation, | 1B | 0 | 1 | 1 | 1 |
|  | 2B | 1 | 0 | 0 | 0 |
|  | 3B | 0 | 1 | 1 | 1 |
|  | 4B | 0 | 1 | 1 | 1 |
|  | 5B | 0 | 1 | 1 | 1 |
|  | 6B | 0 | 1 | 1 | 1 |
|  | 7B | 1 | 0 | 0 | 0 |
| Third channel designation character. | 1 C | 1 | 0 | 0 | 0 |
|  | 2 C | 1 | 0 | 0 | 0 |
|  | 3 C | 0 | 1 | 1 | 1 |
|  | 4 C | 0 | 1 | 1 | 1 |
|  | 5 C | 0 | 1 | 1 | 1 |
|  | 6C | 0 | 1 | 1 | 1 |
|  | 7 C | 1 | 0 | 0 | 0 |

(2) Position the POWER switch on the variable frequency and voltage source (CML N5000A) to ON and allow a 5 -minute warmup.
(3) Position the HIGH VOLTAGE switch on the variable frequency and voltage source to ON.
(4) Adjust the OUTPUT LEVEL control on the variable frequency and voltage source to produce a reading of 120 VAC on the OUTPUT VOLTAGE meter. Adjust the frequency control for 60 CPS.
(5) Position the 115 VAC circuit breaker
switch on the test set to ON and verify that the test set AC on lamp lights.
(6) With current limiting controls set fully clockwise, check that test set dc power supplies are supplying proper voltage output levels-

$$
\begin{aligned}
& \text { +4.75 VDC + 0.1 VDC } \\
& \text { +12.0 VDC + O. } 1 \mathrm{VDC} \\
& \text { - 12.0 VDC + 0.1 VDC }
\end{aligned}
$$

(7) Press the AC POWER switch on the paper tape reader (PTR) and verify that the switches and indicators light as follows:

| AC POWER switch ------ WhiteDC POWER indicator ---- WhiteSTOP switch ----------- RedNOT ASSIGNEDindicator.TAPE |
| :---: |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |

(8) Verify that the reader mechanism motor is operating.
(9) Verify that the blower in the PTR cabinet is operating.
(9.1) Set the TIG ON-LINE/OFFLINE switch to OFF-LINE and observe TIG on indicator is not lit.
(10) Press the paper tape reader AC POWER switch and verify the following results:
(a) No PTR switches or indicators are illuminated.
(b) Reader mechanism drive motor is not operating.
(c) Blower in PTR cabinet is not operating.
(11) Remove the two 15 VAC LAMP fuses from the PTR power supply.
(12) Press the AC POWER switch on the PTR and verify the following results:
(a) Paper tape reader DC POWER indicator illuminates, but all other indicators and switches are out.
(b) Reader mechanism drive motor is operating.
operating.
(c) Blower in PTR cabinet is
(13) Press the paper tape reader AC POWER switch and replace the 15 VAC LAMP fuses.
(14) Remove the 120 VAC 10 A DRIVE MOT fuse from the PTR power supply.
(15) Press the AC POWER switch on the PTR and verify the following:
(a) AC POWER switch, DC POWER indicator, STOP switch, and either HIGH SPEED or LOW SPEED indicators are lit.
(b) Blower in PTR cabinet is operating.
(c) Reader mechanism drive motor is not operating.
(16) Press the AC POWER switch on the PTR and replace the DRIVE MOT fuse.
(17) Remove the 120 VAC 8 A FAN fuse from the PTR power supply.
(18) Press the AC POWER switch and verify the following:
(a) AC POWER switch, DC POWER indicator, STOP switch, and either HIGH SPEED or LOW SPEED indicators are lit.
(b) Reader mechanism drive motor is operating.
(c) Blower in PTR cabinet is not operat-
ing.
(19) Press the AC POWER switch on the PTR and replace the FAN fuse.
(20) Remove the 120 VAC PWR SUP INPUT fuse from the PTR power supply.
(21) Press the AC POWER switch on the PTR and verify the following:
(a) No switches or indicators on the PTR are illuminated.
(b) Reader mechanism drive motor is not operating.
(c) Blower in PTR cabinet is not operating.
(22) Replace the PWR SUP INPUT fuse and remove the + 4.75 VDC fuse.

## NOTE

Following depression of the AC POWER switch (23) below, the drive mechanism motor may run and the blower may operate, and switches and indicators may light momentarily until the power supply shuts off. The conditions of (23) (a) through (c) below 'should be observed within 7 seconds after the AC POWER switch is operated.
(23) Press the AC POWER switch on the PTR and observe the following:
(a) No switches or indicators on the PTR are illuminated.
(b) Reader mechanism drive motor is not operating.
(c) Blower in PTR cabinet is not
operating.
(24) Replace the +4.75 VDC fuse in the power supply.
(25) Remove the +12 VDC, -12 VDC and -48 VDC fuses from the power supply, one at a time, repeating (23) above each time.
(26) With all fuses installed in the power supply, press the AC POWER switch on the PTR. Verify that the AC POWER switch, DC POWER indicator, STOP switch, and either HIGH SPEED or LOW SPEED indicators are lit. Drive mechanism motor should be running and blower in PTR cabinet should be operating.
(27) Set the ASCII/ITA No. 2 switch on the PTR maintenance panel to the ASCII position.
(28) Extend the logic assembly from the PTR cabinet and connect the input of the frequency counter to XA1-T. Adjust the frequency counter to measure a frequency of 9.6 kHz . Frequency should be $9.6 \mathrm{kHz}+1$ percent. (Refer to adjustment, para P66.)
(29) Remove test leads and return logic assembly to the closed position. Close doors on PTR cabinet.
(30) Adjust the PTR tape guides for 1 -inch tape width.
b. Lamp Test. Press the LAMP TEST switch on the control panel of the PTR and verify that the following indicators light:

Switch/Indicator Color

| NOT ASSIGNED ----------- | Amber |
| :---: | :---: |
| TIGHT TAPE .--------------- | Red |
| TAPE OUT ------------------ | Red |
| MOTION FAIL -------------- | Red |
| INVALID CHARACTER --- | Red |
| CANCEL --------------------- | Red |
| START ------------------------ | White-green |
| STOP -------------------------- | Red |
| LOCAL TEST --------------- | Amber |
| SINGLE FEED --------------- | White |
| PILOT HEADER | Amber |
| HIGH SPEED --------------- | White |
| LOW SPEED --- | White |
| AUDIBLE RESET ----------- | Not |

## NOTE

The AC POWER and DC POWER indicators will remain white during the test. They are not tested by the LAMP TEST pushbutton switch.
c. Not Assigned Operation.
(1) Tape slewing. Place a test
sample
(sample D) of punched paper tape in position in
the PTR read head (refer to tape loading procedure of para 2-4. Verify that the TAPE OUT indicator on the PTR is out. Release the slewing lever and insure that the tape can be moved in either direction.
(2) Printed character indexing.
(a) Manually slew the tape until the printed character A appears in the indexing window of the PTR tape cover.
(b) Return the slewing lever to the normal position. Check that the tape is locked in place. Open the tape cover and verify that the punched code for the character A appears over the reader star wheels (refer to fig. 3-3 for punched codes).
(c) Replace test sample D with test tape sample E.
(d) Operate the slewing lever and manually slew the tape until the printed character A is positioned next to the indexing edge of the tape cover on the right-hand side of the cover as viewed from the front.
(e) Return the slewing lever to the normal position. Open the tape cover and verify that the punched code for the character A appears over the reader star wheels.
(3) Speed selection.
(a) Press the HIGH SPEED/LOW SPEED switch on the PTR until the HIGH SPEED position lights white. Verify that the upper half of the switch lights white and the lower half (LOW SPEED) is out.
(b) Press the HIGH

SPEED/LOW SPEED switch once. The top half (HIGH SPEED) should go out and the lower half should light white.
(4) Single feed.
(a) Replace test tape sample E with test tape sample $A$.
(b) Press the SINGLE FEED switch several times and verify that the tape advances one character position each time the switch is pressed. Verify that the STOP switch stays lit and the SINGLE FEED switch is not illuminated after each tape advance.
(c) Press the HIGH

SPEED,/LOW SPEED switch to light the HIGH SPEED portion.
(5) Local test operation.
(a) Press the LOCAL TEST switch and verify that tape advances continuously through the read head at the high speed rate. Verify that the -LOCAL TEST switch illuminates amber and the STOP switch is extinguished simultaneously
when the LOCAL TEST switch is pressed. Verify all other indicators remain unchanged.
(b) Press the HIGH SPEED/LOW SPEED switch to the LOW SPEED position. Observe that the tape moves through the read head at the low speed rate.
(c) While the tape advances, individually press the START, PILOT HEADER, and SINGLE FEED switches. For each switch actuation, verify that all controls and indicators remain unchanged.
(d) Press the STOP switch and verify that the STOP switch illuminates red. Verify that the LOCAL TEST switch indication is extinguished and that the tape stops moving through the read head.
(6) Not assigned RCS Mode.
(a) Replace test tape sample A with test tape sample C. Position the tape in the read head so that the tape starts at the indicated start position.
(b) Press the PTR START switch and verify the following:

1. START switch illuminates green, and STOP indication extinguishes.
2. PTR steps through the sequence of "idle" characters and stops at the end of the sequence with the START and STOP switch indications unchanged from 1 above.
3. The test set READY lamp is not illuminated while the PTR steps through the tape, and test set READY lamp illuminates green when the PTR stops stepping.
4. Verify that the PTR stopped on the first character which is not an "idle" character by noting that the indexing mark on the tape is at the indexing edge of the tape cover.
(7) Start condition switch interaction.
(a) With the START switch and test set READY lamp illuminated green, press the SINGLE FEED, LOCAL TEST, and PILOT HEADER switches. Verify that this has no effect on the PTR or test set.
(b) Press the PTR STOP switch.

Verify that the STOP switch illuminates red, the START switch indication is extinguished, and all other controls and indicators remain the same. Verify that the test set READY indicator is extinguished.
d. Assigned Operation.

Waveforms.
(1) Data Line and Strobe
(a) Replace test tape sample C with test tape sample $P$.
(b) Connect test set DATA LINE TEST

POINT 1 to channel A input of oscilloscope. Trigger the oscilloscope internally on the pulse to be observed and adjust the oscilloscope controls to observe a waveform as shown in figure 6-6.
(c) Press the START switch on the PTR. Press the START switch on the test set and observe the pulse displayed on the oscilloscope. Pulse displayed should have the following parameters:

High level ------------------ +6.0 +0.1
VDC

usec
Fall time ------------------------ 21 to 35
usec
(d) Connect the channel A input of the oscilloscope to the test set DATA LINE TEST POINTS 2 through 7, and the P (parity) test points in numerical sequence. Verify that the pulses displayed meet the parameters listed in
(c) above.
(e) Connect the channel A input of the oscilloscope to the test set STROBE test point.

Verify that the strobe pulse also meets the parameters listed in (c) above.
(f) Connect the channel A input of the oscilloscope to the test set DATA LINE TEST POINT 1, and connect the channel $B$ input of the oscilloscope to the STROBE test point. Set the oscilloscope controls for chopped operation, using the data pulse as an external trigger. Verify that the position of the strobe pulse relative to the data pulse conforms to the limits shown in figure 6-7
(g) Set the test set SELECT switch to ON.
(h) Connect channel A input of oscilloscope to the SELECT test point. Verify a voltage reading of $0.5+0.5 \mathrm{VDC}$.
(i) Place the test set SELECT switch to the off position. Oscilloscope should indicate $6.0+1.0 \mathrm{VDC}$.
(j) Replace test tape sample $P$ with test tape sample $A$.
(k) Set the test set SELECT switch to ON.
(1) Press the HIGH SPEED/LOW SPEED switch on the PTR to the HIGH SPEED position.
(m) Connect oscilloscope channel A input to the READY test point on the test set. Oscilloscope should indicate $0.5+0.5$ VDC.
(n) Press the STOP switch on the paper tape reader. Oscilloscope should indicate 6.0 +1.0 VDC.
(o) Press the START switch on the PTR. Verify that both the PTR START


Figure 6-6. Data pulse and data strobe waveform.
switch and the test set READY lamp illuminate green.
(p) Press the START switch on the test set. Verify that the PTR START switch lights white as the tape advances through the read head, and that the tape stops at a predetermined pattern. Verify that when the tape stops moving, the pattern displayed on the test set COMPARATOR INPUTS indicators is as follows:

$$
\frac{\mathrm{P}}{\mathrm{ON}} \quad \stackrel{7}{\underline{O} N} \frac{6}{\mathrm{O}} \frac{5}{\mathrm{~N}} \quad \frac{4}{\mathrm{OFFF}} \stackrel{3}{\mathrm{O} F F} \stackrel{2}{\underline{O}} \stackrel{1}{\frac{1}{O}}
$$

(q) Press the paper tape reader

STOP switch.
(r) Disconnect the oscilloscope from the STROBE test point and DATA LINE TEST POINTS on the test set. Connect channel A of the oscilloscope to the STEP test point.
(s) Press the START switch on the PTR.
(t) Press the test set START switch.
(u) Verify that the signal levels observed on the oscilloscope are polar, with a nominal +6 VDC high level and a nominal -6 VDC low level.
(v) Press the paper tape reader STOP switch and disconnect the oscilloscope.
(2) Test set search operation.

NOTE
The purpose of the test set search operation is to establish a reference character for both the test set and the PTR under test. Data comparison is then started from this reference character.
(a) Set the ASSIGN/NOT

ASSIGN switch on the test set to ASSIGN.
(b) Connect input A of oscilloscope to ASSIGN test point on test set. Position oscilloscope controls to observe a dc level and verify a reading of $0.5+0.5 \mathrm{VDC}$.
(c) Place the test set

ASSIGN/NOT AS-
SIGN switch to the NOT ASSIGN position.
Os-
1.0
cilloscope should indicate a dc level of $6.0+$
VDC.
(d) Return

ASSIGN/NOT
ASSIGN switch on test set to ASSIGN position. Verify that voltage level returns to level of (b) above, and NOT ASSIGNED indicator on PTR is extinguished.
(3) ASCII data comparison, high speed.


Figure 6-7. Data strobe versus data pulse timing.
(a) Set the test set SEARCH/TEST switch to TEST.
(b) Connect the input of the frequency counter to the STROBE test point on the test set. Position controls on frequency counter to measure a pulse rate of approximately 150 PPS.
(c) Press the test set START switch. Verify that the following actions occur:

1. The test set ALM STOP, OP ALM, and ERROR indicators are all extinguished.
2. Tape moves continuously through the PTR read head.
3. The pattern displayed on the test set data lamps changes continuously, indicating transfer of data from the PTR to the test set.
(d) Verify that frequency counter reads a minimum of 150 pulses per second. Remove frequency counter leads from test set.
(e) Allow the tape to run for 3 minutes
while the procedure of $(\mathrm{f}),(\mathrm{g})$ and (h) below is followed. Verify that no data errors occur during this time. (If a data error does occur, the PTR will stop with the test set ERROR lamp on.)
(f) During the 3-minute run of (e) above, press the LAMP TEST switch on the PTR several times. Verify that the PTR continues to transfer data to the test set without a stop or data error.
(g) During the 3-minute run of (e) above, also press the following switches and verify that pressing the switches has no effect.
```
SINGLE FEED
LOCAL TEST
PILOT HEADER
```

(h) During the 3-minute run of (e) above, press the paper tape reader STOP, paper tape reader START, and test set START switches in
sequence. After performing this operation, verify that the PTR continues to run and data comparison still occurs for the remainder of the 3-minute run.
(i) At the conclusion of (h) above, press the PTR STOP switch.
(j) Press the PTR SINGLE FEED switch. Verify that the STOP switch is extinguished and the SINGLE FEED switch illuminates white. Verify that the test set READY lamp is illuminated.
(k) Press the test set START switch and verify the following:

1. The PTR advances the tape one character.
2. The PTR SINGLE FEED switch indication is extinguished and the STOP switch is illuminated.
3. The test set comparator inputs indicators change pattern showing that a new data character was accepted.
4. The test set ERROR lamp is
not illuminated.
not illuminated.
5. The test set READY lamp is
(I) Repeat (j) and (k) above five times. Verify that data is transferred to the test set without error.
(4) ASCII data comparison, low speed.
(a) Press the PTR HIGH SPEED/LOW SPEED switch to the LOW SPEED position.
(b) Connect the input of the frequency counter to the STROBE test point on the test set. Position controls on frequency counter to measure a pulse rate of approximately 20 PPS.
(c) Press the test set START switch. Verify that the following actions occur:
6. The test set ALM STOP, OP ALM, and ERROR indicators are all extinguished.
7. Tape moves continuously through the PTR read head.
8. The pattern displayed on the test set data lamps changes continuously, indicating transfer of data from the PTR to the test set.
(d) Verify that frequency counter reads a minimum of 20 pulses per second. Remove frequency counter leads from test set.
(e) Allow the tape to run for 3 minutes while the procedure of ( f$)$, ( g ) and ( h ) below is followed. Verify that no data errors occur during this time. (If a data error does occur, the PTR will stop with the test set ERROR lamp on.)
(f) During the 3-minute run of (e) above, press the LAMP TEST switch on the PTR several times. Verify that the PTR continues to
transfer data to the test set without a stop or data error.
(g) During the 3-minute run of (e) above, also press the following switches and verify that pressing the switches has no effect:

## SINGLE FEED <br> LOCAL TEST <br> PILOT HEADER

(h) During the 3-minute run of (e) above, press the paper tape reader STOP, paper tape reader START, and test set START switches in sequence. After performing this operation, verify that the PTR continues to run and data comparison still occurs for the remainder of the 3minute run.
(i) At the conclusion of (h) above, press the PTR STOP switch.
(5) Pilot header.
(a) Replace test tape sample A with test tape sample C. Set the test set COMPARATOR switch to off and press the HIGH SPEED/LOW SPEED switch on the paper tape reader to the HIGH SPEED position.
(b) Press the PILOT HEADER switch on the paper tape reader. Verify that the PILOT HEADER switch illuminates amber. Verify that the tape steps through the "idle" characters and stops at the first character (marked) which is not an "idle" character.
(c) Press the paper tape reader STOP switch. Verify that the STOP switch illuminates and the PILOT HEADER switch remains illuminated.
(d) Press the SINGLE FEED switch on the PTR. Verify that the STOP switch indication is extinguished, the SINGLE FEED switch illuminates white, the test set READY lamp illuminates green, and the PILOT HEADER switch remains illuminated.
(e) Repeat (3) (k) above.
(f) Press the PILOT HEADER switch on the PTR. Verify that the STOP switch is extinguished, the test set READY lamp illuminates green, and the PILOT HEADER switch remains illuminated.
(g) Depress the test set START switch. Verify that the tape advances through the read head until the tape-out condition occurs. At this time verify the following:

1. Tape stops in head head.
2. Paper tape reader TAPE

OUT indi-
cator illuminates.
3. Paper tape reader STOP
switch il-
luminates.
4. Paper tape reader PILOT HEADER switch remains illuminated.
5. Test set READY lamp is not illuminated.
6. Test set OP ALM and ALM STOP lamps are not illuminated.
(6) Message tape-characters inhibited after EOM.
(a) Reload test tape sample C. Verify no change in PTR or test set indications.
(b) Place the test set SEARCH/TEST switch to the SEARCH position and the COMPARATOR switch to ON.
(c) Press the paper tape reader START switch. Verify that the PILOT HEADER and TAPE OUT indications on the PTR are extinguished. Verify that the START switch illuminates white and the test set READY lamp illuminates green.
(d) Press the START switch on the test set. Verify that the PTR START switch lights white as the tape advances through the read head, and that the tape stops at a predetermined pattern. Verify that when the tape stops moving, the pattern displayed on the test set COMPARATOR INPUTS indicators is as follows:

(e) Place the test set SEARCH/TEST switch to TEST, the EOB/EOM switch to on (EOB,/EOM position), and the test set SPEED rotary switch to H S VAR.
(f) Press the test set START switch and verify the following:

1. The tape runs completely through the read head to the end of the tape.
2. Beginning with the 50 N's, the tape speed increases, as the PTR steps through the "idle" characters following the 128 characters sequence.
3. While stepping through the "idle" characters, the paper tape reader START switch illuminates green and the test set READY lamp is not illuminated.
4. The tape stops at the end of the tape with the paper tape reader STOP switch illuminated red and the TAPE OUT indicator not illuminated.
5. The character displayed on the test set data lamps is the last character in the pattern sequence preceding the 50 N 's.
(g) Reload test tape sample C.
(h) Using the SINGLE FEED switch, step the tape one character at a time through the
seven "idle" characters in the leader of the tape. Verify that the pattern displayed on the test set COMPARATOR INPUTS indicator lamps does not change demonstrating that no data is transferred to the test set.
(7) ITA No. 2 Data Comparison-
-1-inch tape width.
(a) Replace test tape sample C with test tape sample $F$.
(b) Set the ASCII/ITA No. 2 switch on the PTR maintenance panel to the ITA No. 2 position.
(c) Set the test set controls as follows: ASCII/ITA No. 2 switch to ITA No. 2. SPEED rotary switch to NORM EOB,/EOM switch to OFF
(d) Place the test set SEARCH/,TEST switch to the SEARCH position.
(e) Press the START switch on the PTR. Verify that both the PTR START switch and the test set READY lamp illuminate green.
(f) Press the START switch on the test set. Verify that the PTR START switch lights white as the tape advances through the read head, and that the tape stops at a predetermined pattern. Verify that when the tape stops moving, the pattern displayed on the test set COMPARATOR INPUTS indicators is as follows:


SEARCH/TEST switch to TEST.
(h) Press the test set START switch. Verify that the following actions occur:

1. The test set ALM STOP, OP ALM, and ERROR indicators are all extinguished.
2. Tape moves continuously through the PTR read head.
3. The pattern displayed on the test set data lamps changes continuously, indicating transfer of data from the PTR to the test set.
(i) Allow the tape to run for 3 minutes. Verify that no data errors occur during this time.
(j) Press tape reader STOP switch.
(k) Remove test tape sample F.
(8) ITA No. 2 data comparison-11/ 6 -itnch wide tape.
(a) Adjust the tape guides on the PTR for 11/16-inch wide tape.
(b) Load test tape sample G into the paper tape reader.
(c) Repeat (7) (d) through (j) above.

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(9) ITA No. 2 data comparison-

7/8-inch wide tape.
(a) Replace test tape sample G with test tape sample H .
(b) Repeat
(7)
(d) through
(j) above.
chadless tape.
(10) ITA No. 2 data comparisonwith test tape sample $L$.
(b) Press the paper tape reader HIGH SPEED/'LOW SPEED switch to the LOW SPEED position.
(c) Repeat (7) (d) through (j)
above.
(11) EOM.
(a) Replace test tape sample L with test tape sample $P$.
(b) Connect channel A input of oscilloscope to the EOM test point on the test set.
(c) Place the test set EOM,'EOB switch on (to the EOM,'EOB position).
(d) Position the oscilloscope controls to view a 6 -volt pulse; use the pulse being viewed as an external trigger.
(e) Press the START switch on the paper tape reader.
(f) Press the START switch on the test set and verify that the tape advances.
(g) Verify that the pulse at the EOM test point has a high level of $6.0+1.0 \mathrm{VDC}$ (starting and finishing level) and a low level of $0.5+0.5$ VDC during the pulse time.

## NOTE

The EOM pulse causes the paper tape reader to stop in a START switch green condition. Repeat (f) above as often as necessary to complete the pulse observation.
(h) Press the STOP switch on the paper tape reader.
(12) EOB.
(a) Connect channel A input of the oscilloscope to the EOB test point on the test set.
(b) Position the oscilloscope controls to view a 6 -volt pulse; use the pulse being viewed as an external trigger.
(c) Press the START switch on the paper tape reader.
(d) Press the START switch on the test set and verify that the tape advances.
(e) Verify that the pulse at the EOB test point has a high level of $+6.0 \pm 1.0$ VDC (starting and finishing level), and a low level of $0.5 \pm 0.5$ VDC during the pulse time.

## NOTE

Repeat (d) above as often
as necessary to complete the observation required in this step.
(f) Press the STOP switch on the paper tape reader.
(g) Place the EOB/EOM switch on the test set to the OFF position.
e. Alarm Conditions.
(1) Tight Tape.
(a) Set the PTR tape guides for

1-inch tape width.
(b) Replace test tape sample L with test tape sample J.
(c) Press the PTR HIGH SPEED/LOW SPEED switch to the HIGH SPEED position.
(d) Set the test set SEARCH/TEST switch to the SEARCH position.
(e) Press the START switch on the PTR. Verify that both the PTR START switch and the test set READY lamp light green.
(f) Press the START switch on the test set. Verify that the PTR START switch lights white as the tape advances through the read head, and that the tape stops at a predetermined pattern. Verify that when the tape stops moving, the pattern displayed on the test set COMPARATOR INPUTS indicators is as follows:

(g) Set the test set SEARCH/TEST switch to the TEST position.
(h) Connect channel A input of oscilloscope to the OP ALM test point on the test set.
(i) Manually grasp the trailing end of the tape.
(j) Press the test set START switch to start the tape stepping through the read head.
(k) Hold the trailing end of the tape from moving and allow the PTR to take up tape until the tight tape sensor actuates.
(I) Upon actuation of the tight tape sensor, verify the following:

1. Tape stops in the read head.
2. PTR TIGHT TAPE indicator illuminates.
illuminates.
extinguished.
3. PTR STOP indicator 5. Test set READY and ERROR lamps not illuminated.
4. Test set OP ALM lamp is illuminated.
5. Oscilloscope indicates voltage level of $6.0+1.0 \mathrm{VDC}$.
(m) Release the tape so that the tape is no longer tight.
(n) Press the PTR START switch. Verify the following:
6. PTR TIGHT TAPE indicator is not illuminated.
7. PTR STOP switch is not illuminated.
white.
illuminated.
illuminated.
VDC.
(o) Press the test set START switch. Verify that the tape resumes stepping without causing a data error.
(p) Press the PTR STOP switch.
(2) Tape motion failure.
(a) Replace test tape sample $J$ with test tape sample K .
(b) Place the test set SEARCH/TEST
switch to the SEARCH position.
(c) Repeat (1) (e) and (f) above.
(d) Place test set SEARCH,/'TEST search to TEST position.
(e) Connect channel A input of oscilloscope to ALM STOP test point on test set. Verify oscilloscope indicates $0.5+0.5 \mathrm{VDC}$.
(f) Press the test set START switch to start tape stepping through the read head.
(g) When the PTR tape drive sprocket wheel runs through the torn sprocket holes, verify the following:
8. PTR MOTION FAIL indicator is illuminated. extinguished.
9. PTR STOP switch is illuminated.
10. PTR START switch is
11. Test set ALM STOP lamp is illuminated. illuminated.
12. Test set READY lamp is not
13. The tape stops in the read head with the torn sprocket holes over the sprocket wheel.
14. Oscilloscope indicates $6.0 \pm 1.0$ VAC.
(3) Reset.
(a) Press the RESET pushbutton on the PTR maintenance panel. Verify that this has no effect.
(b) Set the test set ASSIGN/NOT ASSIGN switch to the NOT ASSIGN position. Verify that the NOT ASSIGNED indicator on the PTR illuminates.
(c) Press the RESET pushbutton on the PTR maintenance panel. Verify that the PTR MOTION FAIL indicator is extinguished. Verify that the test set ALM STOP indicator is extinguished.
(d) Set the Test ASSIGN/NOT ASSIGN switch to the ASSIGN position. Verify that the PTR NOT ASSIGNED indicator is not illuminated.
(4) Invalid character.
(a) Remove test tape sample K from the read head and load the PTR with test tape sample B. Place the test set COMPARATOR switch to off. Set the PTR ASCII/ITA No. 2 switch (on the PTR maintenance panel) to the ASCII position. Set the test set ASCII,'ITA No. 2 switch to the ASCII position.
(b) Press the PTR START switch.-Verify that the tape steps to the first character which is not an "idle" character and stops. The double line index mark on the tape is at the indexing edge of the PTR tape cover.
(c) Press the test set START button. Verify that the tape advances and stops with the following conditions present:
15. A single index line is at the indexing edge of the PTR tape cover.
16. PTR INVALID CHARACTER indicator is illuminated.
17. PTR STOP switch is illuminated.
18. PTR START switch is not
illuminated.
illuminated.
19. Test set ALM STOP lamp is
d
20. Test set READY lamp is not illuminated.
(d) Press the PTR START switch. Verify the following conditions present:
21. PTR INVALID CHARACTER indicator is not illuminated.
22. PTR STOP switch is not illuminated.
green.
illuminated.
illuminated.
23. PTR START switch is illuminated fifty-five invalid characters have been detected.
(f) Following the fifty-fifth invalid character stop, press the PTR START switch and the test set START button in that order. Verify that the tape advances to TAPE OUT with no further invalid character stops.
24. Tape Out. Following (4) (f) above, verify the following:
(a) PTR TAPE OUT indicator is
(b) PTR STOP switch illuminated and START switch is not illuminated.
(c) Test set ALM STOP lamp is illuminated and READY lamp is not illuminated.
(d) Press the PTR START switch. Verify that this has no effect.
(e) Open the PTR tape cover and verify that the end of the tape is three to six character spacings from the reading starwheels.
(f) Remove test tape sample B and load test tape sample A into the PTR. Verify that no change in indication takes place at either the PTR or the test set.
(6) Cancel.
(a) Press the PTR START switch. Verify that the PTR START switch illuminates green and that the PTR TAPE OUT and STOP indications are extinguished.
(b) Connect input A of oscilloscope to CANCEL test point on test set. Verify a voltage level of $0.5+0.5 \mathrm{VDC}$.
(c) Press the test set START button. Verify that tape advances continuously through the read head.
(d) Place the test set CANCEL switch to the MANUAL position. Verify the following results:
25. The test tape stops running through the read head.
26. The PTR CANCEL indicator and STOP switch are illuminated. The PTR START switch is not illuminated.
27. The test set ALM STOP lamp is illuminated and the READY lamp is not illuminated.
28. Oscilloscope indicates $6.0+1.0$ VDC.
(e) Place the test set CANCEL switch to the OFF position.
(f) Press the START switch on the paper tape reader. Verify the following results:
29. The paper tape reader START switch is illuminated green and the STOP and CANCEL indicators are extinguished.
30. The test set ALM STOP lamp is extinguished and the READY indicator is illuminated.
(g) Press the STOP switch on the PTR.
(7) Audible reset.
(a) Connect the channel A input of the oscilloscope to TB2-5 in the paper tape reader to measure the audible reset pulse.
(b) Position the oscilloscope controls to view a 6 -volt pulse, and use the pulse being viewed as an external trigger.
(c) Press the AUDIBLE RESET switch
on the paper tape reader as many times as needed to obtain an accurate measurement of the audible reset pulse.
(d) Verify that pulse is $5 \mu \mathrm{sec}$ minimum in duration, with an amplitude of $6.0 \pm 1.0 \mathrm{VDC}$ at its high level (starting and ending level), and $0.5+0.5$ VDC at its low level during the pulse time.
(e) Disconnect oscilloscope.

## 6-9. Operational Tests-Variable Voltage and Frequency

a. Preliminary Procedure. Position the switches on the test set as follows:
115 VAC circuit breaker to ON
CANCEL to OFF
SELECT to ON
SPEED rotary switch to NORM
COMPARATOR INPUT switch to DATA IN
EOB,/EOM to OFF
ASSIGN/NOT ASSIGN to ASSIGN
COMPARATOR to OFF
AUTO/MAN to AUTO
SEARCH/TEST to TEST
ASCIIIITA No. 2 to ASCII
b. Operation With Static Variations of Frequencies and Voltages.
(1) Position variable frequency and voltage controls on CML 5000A to the first ( 132 VAC, 60 CPS) position indicated on the chart below (positions indicated by an "X").

| Test voltage (VAC) | Test frequency (CPS) |  |  |
| :---: | :---: | :---: | :---: |
|  | 57 | 60 | 63 |
| 132-------------------------------- | -- | X |  |
| 120-------------------------------------- | X | X | X |
| 96------------------------------------- | -- | x |  |

(2) Load test tape sample A. (Load with splice up.)

ON.
(3) Set the test set COMPARATOR switch to
(4) Set the test set SEARCH/TEST switch to the SEARCH position.
(5) Press the START switch on the PTR. Verify that both the PTR START switch and the test set READY lamp light green.
(6) Press the START switch on the test set. Verify that the PTR START switch lights white as the tape advances through the read head, and that the tape stops at a predetermined pattern. Verify that when the tape stops moving, the pattern displayed on the test set COMPARATOR INPUTS indicators is as follows:

| P | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ON | OFF | ON | ON | OFF | OFF | OFF | OFF |

(7) Set the test set SEARCH/TEST switch to TEST.

Connect the input of the frequency counter to the STROBE test point on the test set. Position controls on frequency counter to measure a pulse rate of approximately 150 PPS.
(9) Press the test set START switch. Verify that the following actions occur:
(a) The test set ALM STOP, OP ALM, and ERROR indicators are all extinguished.
(b) Tape moves continuously through the PTR read head.
(c) The pattern displayed on the test set data lamps changes continuously, indicating transfer of data from the PTR to the test set. (10) Verify that frequency counter reads 150 +4.5 pps.
(11) Press the STOP switch on the PTR.
(12) Repeat (5) and (8) through (11) above for all remaining settings of frequency and voltage as indicated on an " $X$ " in the chart of (1) above.
(13) Press AC POWER switch on PTR to shut off paper tape reader.
(14) Convert tape reader mechanism from 60 Hertz to 50 Hertz operation by performing the instructions for 50-Hz conversion in TM 11-7440-239-15.
(15) Position variable frequency and voltage controls on the CML 5000A to the first (132 VAC, 50 CPS) position indicated on the chart below (positions indicated by an X ).

| Test voltage (VAC) | Test frequency (CPS) |  |  |
| :---: | :---: | :---: | :---: |
|  | 47.5 | 50 | 52.5 |
| 132----------------------------------- | -- | X |  |
| 120----------------------------------- | X | X | X |
| 96-------------------------------------- | -- | x |  |

(16) Press AC POWER switch on PTR.
(17) Repeat (4) through (7) above.
(18) Repeat (5) and (8) through (11) above for each of the voltage and frequency settings indicated by an $X$ in the chart of (15) above.
c. Dynamic Variable Voltage at 50 Hertz (120 $V A C)$.
(1) Adjust the variable frequency and voltage source for 50 Hertz and 120 VAC.
(2) Press the paper tape reader START switch.
(3) Press the test set START switch.
(4) Vary the OUTPUT LEVEL adjust on the CML N5000A from a nominal 120 VAC to a minimum of 96 VAC, then to a maximum of 132 VAC, and then return to 120 VAC. This cycle should be completed in approximately 60 seconds.
(5) Verify the frequency counter reads $150+4.5$ PPS while voltage is varied.
(6) Press the paper tape reader STOP switch at the end of the cycle.
d. Dynamic Variable Frequency at 120 VAC 50 Hertz).
(1) Press the paper tape reader and test set START switches in sequence.
(2) Vary the FREQUENCY CPS adjust on the CML N5000A from a nominal 50 CPS to a minimum 47.5 CPS, then to a maximum 52.5 CPS, and return to 50 CPS. This cycle should be completed in approximately 60 seconds.
(3) Verify that the frequency counter reads 150 $\pm 4.5$ PPS while frequency is varied.
(4) Press the paper tape reader STOP switch at end of the cycle.
(5) Press AC POWER switch on PTR.
(6) Convert tape reader mechanism from 50 Hertz to 60 Hertz operation again. (Reverse procedure given in TM 11-7440-239-15.)
e. Dynamic Variable Frequency at 120 VAC (60 Hertz).
(1) Adjust the variable frequency and voltage source to 60 CPS and 120 VAC.
(2) Press the AC POWER switch on the paper tape reader.
(3) Repeat $\mathrm{b}(4)$ through (8) above.
(4) Vary the FREQUENCY CPS adjust on the CML N5000A from a nominal 60 CPS to a minimum of 57 CPS, then to a maximum of 63 CPS, and return to 60 CPS. This cycle should be completed in approximately 60 seconds.
(5) Verify that the frequency counter reads 150 $\pm$ 4.5 PPS while frequency is varied.
(6) Press paper tape reader STOP switch at end of cycle.
f. Dynamic Variable Voltage at 60 Hertz.
(1) Adjust the variable frequency and voltage source for 60 CPS and 120 VAC.
(2) Press the PTR and test set START switches in sequence.
(3) Vary the OUTPUT LEVEL adjust on the CML N5000A from a nominal 120 VAC to
a minimum of 96 VAC , then to a maximum of 132 VAC , then return to 120 VAC. This cycle should be completed in approximately 60 seconds.
(4) Verify that the frequency counter reads 150 $\pm 4.5$ PPS while voltage is varied.
(5) Press PTR STOP switch at end of cycle.
g. Dynamic Variable Frequency at 120 VAC ( 60 Hertz) in Low Speed Mode While Reading Chadless Tape.
(1) Remove test tape sample A from the PTR. Position the tape guides for $11 / 16$-inch width tape and load test tape sample L.
(2) Press the paper tape punch HIGH SPEED "LOW SPEED switch to the LOW SPEED position. Set the ASCIIIITA No. 2 switch on the PTR maintenance panel to the ITA No. 2 position. Set the test set ASCII/ITA No. 2 switch to the ITA No. 2 position.
(3) Position the frequency counter controls to read approximately 20 PPS.
(4) Set the OUTPUT LEVEL and FREQUENCY CPS controls on the CML N5000A for 120 VAC and 60 CPS.
(5) Repeat $\mathrm{b}(4)$ through (8) above.
(6) Vary the FREQUENCY CPS adjust on the CML N5000A from a nominal 60 CPS to a minimum of 57 CPS and to a maximum of 63 CPS, then return to 60 CPS. This cycle should take approximately 60 seconds.
(7) Verify that frequency counter reads $18.75 \pm$ 0.5 PPS while frequency is varied.
(8) Press the paper tape reader STOP switch at the end of the cycle.
h. Dynamic Variable Voltage at 60 Hertz (120 TVAC) in Low Speed Mode Reading Chadless Tape.
(1) Press the paper tape reader and test set START switches in sequence.
(2) Vary the OUTPUT LEVEL adjust on the CML N5000A from a nominal 120 VAC to a minimum of 96 VAC, then to a maximum of 132 VAC, and return to the 120 VAC. This cycle should take approximately 60 seconds. (3) Verify frequency counter reads $18.75 \pm 0.5$ PPS while voltage is varied.
(4) Press the paper tape reader STOP switch at end of cycle.
(5) Remove test tape samply $L$ from the paper

## 6-10. Shutdown

a. Press AC POWER switch on paper tape reader.
b. Position 115 VAC circuit breaker on test set to OFF.
c. Position the CML N5000A HIGH VOLTAGE switch to OFF; then place the POWER switch to OFF.
d. Perform the following if you do not have a transmission identification generator to test (para 6-11).
(1) Remove connection between paper tape reader and CML N5000A.
(2) Remove connection between paper tape reader and test set.

## 6-11. Operational Test-Transmission Identification Generator

a. Initial Setup. This test checks for proper operation of a transmission identification generator kit installed on a punched tape reader. It is necessary that a protested punched tape reader meeting the requirements of baragraphs 6-7 through 6-10 be used.
(1) Initial set up. Connect the paper tape reader and the transmission identification generator to the test equipment as shown in figure 6-8.
(2) Place CML N5000A HIGH VOLTAGE switch to ON; then place the POWER switch to ON.
(3) Press the AC POWER switch on the paper tape reader and verify that the AC PON'ER switch and DC POWER indicator light white.
(4) Set the TIG ON-LINE OFF-LINE switch to the ON-LINE position. Verify that the TIG ON indicator is illuminated white.
(5) Verify that the PTR ASCII/ITA-2 switch on the front of the punched tape reader logic assembly is set to the ASCII position.
(6) Verify/set the controls and switches on the paper tape reader test as follows:
CANCEL to OFF
SELECT to OFF
EOB /EOM to ON
SPEED to NORM
ASSIGNED/NOT ASSIGNED to ASSIGNED COMPARATOR INPUT to INPUT REG COMPARATOR to OFF tape reader.


Figure 6-8. Test setup for TIG.

STEP/COUNTER to STEP
AUTO/MAN to MAN
SEARCH/TEST to TEST
ASCII/ITA-2 to ASCII
115 VAC circuit breaker to ON
b. Channel Sequence Number Indicator.
(1) Manually update the channel sequence number for each of the numbers indicated below.
Dial the MANUAL UPDATE thumbwheel switches on the TIG control panel to one of the following numbers and then press the LOAD switch. Observe the proper numbers are shown in the NEXT NUMBER display.

| 111 | 444 | 777 | 000 |
| :--- | :--- | :--- | :--- |
| 222 | 555 | 888 |  |
| 333 | 666 | 999 |  |

(2) Load test tape sample $M$ in the punched tape reader.
(3) Press the AC POWER switch on the punched tape reader twice to turn power off and then back on. Verify that the TIG NEXT NUMBER display is automatically reset to 000 when the AC POWER is turned on.
(4) Manually load 999 into the TIG NEST NUMBER display. Use procedure outlined in (1) above.
(5) Set the test set SELECT switch to ON.
(6) Press the punched tape reader START switch and observe that the START switch lights green.
(7) Press the test set START switch and observe the punched tape reader START switch remains green.
(8) Now attempt to manually load 111 into the NEXT NUMBER display (procedure outlined in (1) above). Observe that you cannot update the display.
(9) Set the test set CANCEL switch to MANUAL. Observe the following indications on the punched tape reader control panel:
START switch is not illuminated.
STOP switch lights red.
CANCEL switch lights red.
(10) Set the test set CANCEL switch to OFF.
(11) Press the punched tape reader START switch. Verify the START switch lights green.
(12) Press the test set START switch 16 times. On the TIG control panel, observe the NEXT NUMBER display advances to 000 .
c. Transmission Identification (TI) Sequence. This section has four TI sequences with special jumper connections on the selection option board on punched tape reader PC card A2 required before each sequence. These sequences have been such that they verify-
Operation of the TIG with the punched tape reader and the test set:
ASCII code odd parity.
Proper data transfer.
TI format.
Programable ACP-127 start of message.
Programable TI channel designation characters.
Channel sequence number.
EM signal generation.
(1) TI sequence number 1 .
(a) Press the punched tape reader AC POWER switch. Verify the AC POWER switch and the DC POWER indicator are not lighted.
(b) Remove PC Card A2 from the punched tape reader logic assembly. Verify that jumper wires are connected on the strapping option terminals as indicated in the TI sequence number column of table 6-5
(c) Replace PC card A2 in the punched tape reader.
(d) Press the punched tape reader AC POWER switch and observe:
AC POWER switch lights white.
DC POWER indicator lights white.
STOP switch lights red.
(e) Load test tape sample $M$ in the middle of the idle characters.
(f) Set the test set SELECT switch to OFF.
(g) Manually load 000 into the TIG NEXT NUMBER display. Use procedure outlined in $\mathrm{b}(1)$ above.
(h) Set the test set SELECT switch to N .
(i) Press the punched tape reader START switch. Observe the following:
The START switch lights green.
The test tape in the punched tape reader advances to the first character of the message and then stops.
(j) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6+1$ VDC.
Test set COMPARATOR INPUTS lights display 11011010 (character Z).
(k) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 01000011 (character C).
(I) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 11011010 (character Z).
(m) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VD} \overline{\mathrm{C}}$.
Test set COMPARATOR INPUTS lights display 01000011 (character C).
( $n$ ) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 11000001 (character A).
(o) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 11000010 (character B).
(p) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 01000011 (character C).
(q) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 00001110 (character SO).
(r) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 10110000 (character 0).
(s) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 10110000 (character 0)
( $t$ ) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 10110000 (character 0).
(u) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 10001111 (character SI).
(v) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 00001101 (character CR).
(w) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC. Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 00001101 (character CR).
(x) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4+1$
VDC.
Test set EM test point measures $+6+1$ VDC.
Test set COMPARATOR INPUTS lights display 10001010 (character LF).
(y) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures a $100 \mu \mathrm{sec}$ wide negative going pulse.
Test set EM test point measures $0 \pm .5$ VDC.
Test set COMPARATOR INPUTS lights display 10000000 (character NUL).
TIG NEXT NUMBER display counts to '001'.
(2) TI sequence number 2.
(a) Press the punched tape reader AC POWER switch. Verify the AC POWER switch and the DC POWER indicator are not lighted.
(b) Remove PC Card A2 from the punched tape reader logic assembly. Change jumper wires to connect the strapping option terminals as indicated in the TI sequence number 2 column of table 65.
(c) Replace PC Card A2 in the punched tape reader.
(d) Press the punched tape reader AC POWER switch and observe-
AC POWER switch lights white.
DC POWER indicator lights white.
STOP switch lights red.
(e) Load test tape sample M in the middle of the idle characters.
(f) Set the test set SELECT switch of OFF.
(g) Manually load 777 into the TIG NUMBER display. Use procedure outlined in $\mathrm{b}(1)$ above.
(h) Set the test set SELECT switch to ON.
(i) Press the punched tape reader START switch. Observe the following:
The START switch lights green.
The test tape in the punched tape reader advances to the first character of the message and then stops.
(j) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS display 010-00011 (character C ).
(k) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 11011010 (character Z).
(I) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display
01000011 (character C).
( $m$ ) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6+ \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 00111110 (character >).
(n) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{~V} \overline{\mathrm{D}} \mathrm{C}$.
Test set COMPARATOR INPUTS lights display 00111101 (character =).
(o) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 10111100 (character <).
(p) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6+1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 00001110 (character SO).
(q) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 00110111 (character 7).
(r) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{~V} \overline{\mathrm{D}} \mathrm{C}$.
Test set COMPARATOR INPUTS lights display 00110111 (character 7).
(s) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6+1 \mathrm{VD} \overline{\mathrm{C}}$.
Test set COMPARATOR INPUTS lights display 00110111 (character 7).
(t) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 10001111 (character SI).
(u) Press the test set START switch one time. Observe the following:
TIG simulator test point TPI measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 00001101 (character CR).
(v) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 00001101 (character CR).
(w) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 100001010 (character LF).
(x) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures a $100-\mu \mathrm{sec}$ wide negative pulse.
Test set EM test point measures $0+.5$ VDC.
Test set COMPARATOR INPUTS lights display 10000000 (character NUL).
TIG NEXT NUMBER display increments to 778.
(3) Tl sequence number 3.
(a) Press the punched tape reader AC POWER switch. Verify the AC POWER switch and the DC POWER indicator are not lighted.
(b) Remove PC Card A2 from the punched tape reader logic assembly. Change jumper wires to connect the strapping option terminals as indicated in the TI sequence number 3 column of table 65.
(c) Replace PC card A2 in the punched tape reader.
(d) Press the punched tape reader AC

POWER switch and observe:
AC POWER switch lights white.
DC POWER indicator lights white.
STOP switch lights red.
(e) Load test tape sample M in the middle of the idle characters.
(f) Set the test set SELECT switch of OFF.
(g) Manually load 889 into the TIG NEXT NUMBER display. Use procedure outlined in $\mathrm{b}(1)$ above.
(h) Set the test set SELECT switch to ON.
(i) Press the punched tape reader START switch. Observe the following:
The START switch lights green.
The test tape in the punched tape reader advances to the first character of the message and then stops.
(j) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 11011010 (character Z).
(k) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 01000011 (character C).
(I) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VD} \overline{\mathrm{C}}$.
Test set COMPARATOR INPUTS lights display 00111110 (character >).
( $m$ ) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 00111101 (character $=$ ).
( $n$ ) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC. Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 10111100 (character<).
(o) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 00001110 (character SO).
(p) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.

Test set COMPARATOR INPUTS lights display 00111000 (character 8).
(q) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPŪTS lights display 00111000 (character 8).
(r) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 10111001 (character 9).
(s) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 10001111 (character SI).
(t) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 00001101 (character CR).
(u) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1 \mathrm{VDC}$.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$. Test set COMPARATOR INPUTS lights display 00001101 (character CR).
(v) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUT̄S lights display 10001010 (character LF).
(w) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures a $100 \mu \mathrm{sec}$ wide negative pulse.
Test set EM test point measures $0 \pm .5$ VDC.
Test set COMPARATOR INPUTS lights display 10000000 (character NUL).
TIG NEXT NUMBER display increments to '890'.
(4) TI sequence number 4.
(a) Press the punched tape reader AC

POWER switch. Verify the AC power switch and the DC POWER indicator are not lighted.
(b) Remove PC Card A2 from the punched tape reader logic assembly. Change jumper wires to connect the strapping option terminals as indicated in the TI sequence number 4 column of table 65.
(c) Replace TC Card A2 in the punched tape reader.
(d) Press the punched tape reader AC

POWER switch and observe:
AC POWER switch lights white.
DC POWER indicator lights white.
STOP switch lights red.
(e) Load test tape sample M in the middle of the idle characters.
(f) Set the test set SELECT switch to

OFF.
(g) Manually load 899 into the TIG NEXT NUMBER display. Use procedure outlined in $\mathrm{b}(1)$ above.
(h) Set the test set SELECT switch to ON.
(i) Press the punched tape reader START
switch. Observe the following:
The START switch lights green.
The test tape in the punched tape reader advances to the first character of the message and then stops.
(j) Press the test set START switch one
time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 01000011 (character C).
(k) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 00111110 (character>).
(I) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 00111101 (character $=$ ).
( $m$ ) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.

Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 10111100 (character <).
(n) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 00001110 (character SO).
(0) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 00111000 (character 8).
(p) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 10111001 (character 9).
(q) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 10111001 (character 9).
(r) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPŪTS lights display 10001111 (character SI).
(s) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1 \mathrm{VD} \overline{\mathrm{C}}$.
Test set COMPARATOR INPUTS lights display 00001101 (character CR).
( t ) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures $+4 \pm 1$ VDC.
Test set EM test point measures $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 00091101 (character CR).
(u) Press the test set START switch one time. Observe the following:

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TIG simulator test point TP1 measures $+4 \pm 1$ VDC. Test set EM test point measures $+6 \pm 1 \mathrm{VD} \overline{\mathrm{C}}$.
Test set COMPARATOR INPUTS lights display 10001010 (character LF).
(v) Press the test set START switch one time. Observe the following:
TIG simulator test point TP1 measures a $100 \mu \mathrm{sec}$ wide negative pulse.
Test set EM test point measures $0+ \pm .5 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 10000000 (character NUL).
TIG NEXT NUMBER display counts to 900.
d. Off-Line Operation of EM Interface Signal.
(1) Set the TIG ON-LINE,/OFF-LINE switch to the OFF-LINE position.
(2) Load test tape sample $M$ in the middle of the idle characters.
(3) Set the test set CANCEL switch to the MANUAL position.
(4) Set the test set CANCEL switch to the OFF position.
(5) Press the punched tape reader START switch. Verify the START switch lights green.
(6) Press the test set START switch one time. Observe the following:
Test set EM test points remains at $+6 \pm 1 \mathrm{VDC}$.
Test set COMPARATOR INPUTS lights display 01010100 (character T).
(7) Press the test set START switch one time. Observe the following:
Test set EM test point remains at $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 11001000 (character H).
(8) Press the test set START switch one time. Observe the following:
Test set EM test point remains at $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 01001001 (character I).
(9) Press the test set START switch one time. Observe the following:
Test set EM test point remains at $+6- \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 11010011 (character S).
(10) Press the test set START switch one time. Observe the following:
Test set EM test point remains at $+6 \pm 1$ VDC.
Test set COMPARATOR INPUTS lights display 00100000 (character SPACE).
e. Incrementing by Other TIG Press the push-
button on the TIG simulator several times. Verify the TIG NEXT NUMBER display is incremented by one each time the simulator pushbutton is pressed and released.
$f$. Verification of Error Free Operation.
(1) Set the test set AUTO/MAN switch to the AUTO position.
(2) Set the TIG ON-LINE/OFF-LINE switch to the ON-LINE position.
(3) Load test tape sample $M$ in the middle of the idle characters.
(4) Manually load the TIG NEXT NUMBER indicator to 000.
(5) Press the START switch on the paper tape reader. Observe test tape advances to the first valid character on the tape and then stops.
(6) Press the START switch on the test set. Observe that one message is processed by the paper tape reader. Verify that the TIG NEXT NUMBER indicator is incremented by one.
(7) Repeat (6) above nine times (until the TIG NEXT NUMBER indicator displays 010).
(8) Repeat (6) above one time after manually loading each of the following numbers in the TIG NEXT NUMBER indicator.
Verify the TIG NEXT NUMBER indicator is incremented by one each time a message is processed.

| 019 | 069 | 199 | 699 |
| :--- | :--- | :--- | :--- |
| 029 | 079 | 299 | 799 |
| 039 | 089 | 399 | 899 |
| 049 | 099 | 499 | 999 |
| 059 |  | 599 |  |

## 6-12. Shutdown

a. Press the AC POWER switch on the paper tape reader.
b. Position the 115 VAC circuit breaker on test set to OFF.
c. Position the CML N5000A HIGH VOLTAGE switch to OFF; then place the POWER switch to OFF.
d. Disconnect the TIG simulator from TIG assembly.
e. Remove the connection between the paper tape reader and the CML N5000A.
$f$. Remove the connection between the paper tape reader and the test set

## CHAPTER 8

 ILLUSTRATIONS

Fiqure 8-6(2). Reader mechanism assembly A2, schematic diagram (part 2 of 2).


Figure 8-9. PC card A4 (No. A65215-001), schematic diagram.


FOR PUNCHED TAPE READERS HAVING TIG asSEMBLY a7 OR a8 INSTALLED, REFER TO FIGURE 8-9.3.

Figure 8-9.1. PC card A4 (No. A65223-001), schematic diagram.
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Figure 8-9.2. PC card A4 (No. A65215-001), schematic diagram. (with TIG installed)

Change 4 8-28.1


Figure 8-9.3. PC card A4 (No. A65223-001),schematic diagram. (with TIG installed)

Change 4 8-28.2


FOR PUNCHED TAPE READERS HAVING TIG ASSEMBLY A7 OR A8 INSTALLED, REFER TO FIGURE 8-10.2.


| POWER INPUT PINS |  |  |
| :---: | :---: | :---: |
|  | $Z 10$ | ZI THRU Z9 |
| +4.5 VOC | 6 | NOT USED |
| GRD | 1 | 7 |
| +12 VOC | NOT USED | 13 |
| -12 VDC | NOT USED | 1 |

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Figure 8-10.1. PC card A5 (No. A65227-001), schematic diagram
Change 4 8-30.1


| POWER INPUT PINS |  |  |
| :---: | :---: | :---: |
|  | 210 | 21 THRU 29 |
| +4.5 VOC | 6 | NOT USED |
| GRD | 1 | 7 |
| +12 VOC | NOT USED | 13 |
| -12 VOC | MOT USED | 1 |

Figure 8-10.2. PC card A5 (No. A65227-001), schematic diagram.
(with TIG installed)
Change 4 8-30.2

LOGIC ASSEMBLY AI（WITHOUT T．I．G．）WIRE LIST

|  | FROM | TO | FROM | TO | FROM | TO | FROM | TO |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | IN－PIN | CON－PIN | CON－PIN | CON＝PIN | CON－PIN | COV－PIN | CON－PIN | CLiv－PIN |
|  | 1 | $187-78$ | J 3－AA | F 3 | THIH－01 | xa15－01 | XA 4－07 | J 1－14 |
|  | 1 | J $1-4 \mathrm{~A}$ | J 3－01 | J 2－01 | T81H－i） | xA15－${ }^{\text {a }}$ | XA 4－35 | xa 15－2） |
|  | 2 | J 2－AA | 」 3－01 | J 3－05 | TB1H－02 | XA15－0？ | XA 4－09 | J 1－2 |
|  | 3 | J 3－AA | J 3－03 | XA 7－18 | TblJ－01 | S 1－C | XA 4－19 | XA15－C |
|  | 4 | J $¢-1 / 4$ | J 3－05 | 」 3－01 | TR1J－OL | 5 2－0， | XA 4－11 | J 1－ |
|  | 1－1 | x 4 4－21 | J 3－05 | 」 3－01 | 151J－02 | S 2－01 | X4 4－1？ | x 415－17 |
|  | 1－N | K $\mathrm{AS}_{4}$－14 | J 3－0t | J 3－05 | $\times 4$ 1－A | 1A1A－01 | XA 4－13 | J $1-x$ |
|  | $1-$ | x 4 －E | J 3－07 | 」 3－09 | $\times 1$ 1－A | 」 2－01 | x4 4－14 | J 1－＇d |
|  | 1－T | xA 4－11 | 」 3－09 | J 3－C7 | XA 1－B | J 2－02 | XA $4-10$ | xalb－us |
|  | $1-\mathrm{V}$ | XA 4－05 | J 3－09 | J 3－1t | $\times \mathrm{A} 1-\mathrm{B}$ | TBla－02 | XA 4－17 | J 1－21 |
|  | $1-X$ | XA 4－13 | J 3－11 | J 3－09 | XA 1－C | TA $2-1 \mathrm{~B}$ | XA 4－15 | XA15－f |
|  | 1－ 7 | X $\wedge$ 4－179 | J 3－11 | J 3－13 | XA 1－C | J 4－C | XA 4－19 | J 1－2 |
|  | 1－4A | F 1 | J 3－13 | J 3－11 | XA 1－C | Xa 3－C | XA 4－20 | XA1b－0．3 |
|  | 1－61 | XA S－${ }^{1}$ | 」 3－13 | J 3－15 | $\times \mathrm{A}$ 1－？ | XA14－0 | XA 4－21 | J 1－1 |
| J | 1－03 | XAS－V | J 3－15 | J 3－13 | $\times \mathrm{A}$ 1－ 1 | XA14－14 | XA 4－2？ | $\times 4$ 4－04 |
| J | 1－05 | $\times \wedge 5-X$ | J 3－15 | 」 3－17 | $\times x^{\text {a }} 1-01$ | J 3－22 | XA 4－72 | XA15－12 |
| J | 1－17 | XA 5－27 | J 3－17 | J 3－15 | XA 1－01 | J 3－A |  | xal6－21 |
|  | $1-39$ | $\times$－5－${ }^{1}$ | J 3－17 | J 3－19 | $\times 4$ 1－i82 | T®1A－02 | $X A 5-A$ | Tilc－il |
|  | 1－11 | XAS－F | J 3－19 | J 3－17 | XA 1－03 | 18 2－20 | XA 5－A | xA 6－A |
|  | 1－13 | XA 5－H | J $3-19$ | J 3－21 | $x$（ $1-03$ | xA 3－03 | XA 5－ 5 | Tuic－02 |
|  | 1－15 | $X A$ S－J | J 3－21 | J 3－19 | X4 1－05 | J 4－1 | XA 5－ 5 | XA b－${ }^{\text {¢ }}$ |
|  | 1－17 | $x$ x 5－12 | 」 3－22 | J 2－A | KA 1－06 | J 4－L | XA $\mathrm{XA}^{\text {－}}$（ | $\times 4$ 4－C |
| J | 1－19 | X $\times 4-17$ | J 3－22 | XA 1－01 | $\times$ ¢ 1－0B | In 2－4H | $\times \mathrm{A} 5-\mathrm{C}$ | $\times$ ¢ 7－C |
|  | 1－？ 1 | XA 4－17 | $\mathrm{J}+\mathrm{C}$ | TB 2－18 | $\times 41-09$ | TH 2－4 A | XA 5－0 | d ：－ix9 |
|  | 1－3 3 | 人A 4－19 | J 4－C | J 2－C | $\times$ x 1－10 | 18 2－30 | XA 5－ |  |
|  | 2－A | J $3-22$ | J 4－C | XA 1－C | $x^{\prime}$ A $1-10$ | J 4－10． | XA 5－： | J 1－11 |
|  | 2－A | J 3－0 | J 4－1 | $\times 41-05$ | MA 1－14 | XA15－u9 | XA 5－11 | J 1－13 |
|  | 2－C | J $7-04$ | J 4－1 | XA 1－0t | XA 3－${ }^{\text {a }}$ | TH 2－58 | XA 5－J | J 1－15 |
|  | 2－C | J 4 －C | J $4-A A$ | $\pm 4$ | XA 3－C | XA 1－C | XA S－K | XA 6－05 |
|  | －-1 | XA15－23 | J 4－10 | XA 1－10 | XA 3－C | XA 4－C | XA 5－L | $x A 6-21$ |
|  | 2－H | XA1G－K | S 1－C | TH1J－01 | XA 3－D | X414－08 | XA 5－U | J 1－01 |
|  | 2－J | XA16－A4 | 5 1－NT | X415－10 | $\times \mathrm{A}$ 3－E | x416－06 | XA 5－V | J 1－0．1 |
| J | 2－K | $X A 1 B-12$ | S 2－01 | 5 2－06 | $\times \mathrm{A}$ 3－F | J 2－U | XA 3－w | XA 6－15 |
|  | $7-$ | XA1S－11 | $5 \quad 2-01$ | 541J－02 | XA 3－F | XA14－V | XA 5－$X$ | J 1－i） |
|  | 3－4 | XA1S－18 | S 2－02 | XA 7－11 | XA 3－ H | XA15－04 | XA5－Y | XA 0－${ }^{\text {－}}$ |
|  | 2－N | XAlt－1 | 5 2－03 | THLJol | XA 3－J | XAlb－M | XA 5－1 | $x$ ¢ $\quad$－$\times$ |
|  | 2－p | XA1：－17 | S 2－0．3 | 5 2－04 | XA 3－K | xal6－Y | XA 5－31 | Tnic－ut |
| $J$ | 2－ | XA1S－R | S $7-04$ | 5 2－03 | $\times \mathrm{A}$－ R | J 2－11 | XA $5-01$ | $\times 4$ 6－01 |
|  | 2－1 | $\times 4$ 3－19 | S 2－05 | xa 7－ma | $\times 4$ 3－ 5 | J 2－06 | X4 5－07 | THIC－02 |
|  | p－u | XA3－5 | S 2－06 | 5 2－01 | XA 3－1 | J 2－09 | XA 5－02 | XA 6－02 |
|  | 7－v | XA 3－22 | Tb 1－01 | $183-18$ | $x \wedge 3-U$ | J 2－16 | XA 5－3） | xA 4－03 |
|  | ？－ | XALS－ | TH 1－02 | T8 3－28 | $\times \mathrm{A} 3-\mathrm{V}$ | J 2－17 | XA 5－07 | XA 7－10 |
| J | $2-x$ | $X A 16-22$ | 14 $\boldsymbol{1}$－18 | J 4－C | $\times \mathrm{A} 3-\mathrm{W}$ | 」 2－12 | XA 5－1： | $\times \mathrm{A} 4$－vo |
|  | $2-A A$ | F 2 | 1B 7－18 | XA 1－C | $x \wedge$ 3－$X$ | J 2－20 | XA 5－10 | xA15－16 |
|  | 7－11 | 」 3－01 | TH 2－2B | XA 1－03 | XA 3－$Y$ | J 2－15 | XA 5－11 | xA 5－17 |
|  | 7－71 | $\times \mathrm{A} 1-\mathrm{A}$ | TE 2－30 | $\times 41-10$ | XA 3－01 | TB ？－54 | $x$ A 5－1？ | J 1－17 |
|  | 2－02 | XA 1－B | 18 2－48 | XA 1－08 | $\times$ x 3－01 | J ？ 214 | XA 5－13 | XA 5－11 |
|  | 2－04 | J 2－C | T8 2－4日 | $\times 41-09$ | XA 3－03 | x4 1－03 | xA 5－14 | xA14－0n |
|  | 2－nob | XA 3－5 | TS 2－58 | XA 3－A | XA 3－03 | $X_{A} 4-03$ | $\mathrm{xA} 5-7.7$ | J 1－07 |
|  | 1－97 | $\times 4$ 3－15 | 厂如 2－5 | XA 3－01 | XA 3－04 | J 2－08 | XA 5－21 | XA 6－ |
|  | 2－bid | XA 3－04 | Ts 2－78 | E 1 | $x$ x 3－05 | 」 2－07 | XA 6－A | $\times$－5－ 1 |
|  | ＜－09 | $\times \mathrm{A} 3-1$ | TH 3－1H | TR 2－01 | XA 3－06 | J 2－13 | XA 6－${ }^{\text {¢ }}$ | XA 5－ 4 |
|  | 2－10 | $\times 4 \geq-199$ | TH 3－28 | 18 1－02 | XA 3－07 | J 2－18 |  | $x_{A}$ 5－21 |
|  | 2－11 | XA 3－R | TH1A－01 | J 3－ 4 | XA 3－00 | J 2－19 | XA 6－ | XA 7－P |
|  | 2－12 | $\times \mathrm{A} 3-\mathrm{W}$ | TR14－01 | $x$ ¢ 1－4 | XA 3－09 | J 2－10 | XA 6－w | $X A 5-Y$ |
|  | 7－13 | XA 3－136 | TH1A－07 | XA 1－${ }^{\text {a }}$ | XA 3－14 | XAlS－H | XA G－${ }^{\text {W }}$ | XA 7－Y |
|  | 2－14 | XA 3－01 | TR1A－02 | XA 1－02 | XA 3－15 | XA16－14 | XA G－$X$ |  |
|  | 2－15 | XA 3－Y | T81R－01 | xa 4－F | XA 3－16 | XA16－03 | XA G－X | ＜A 7－N |
|  | 2－16 | XA 3－U | TA1d－01 | XA 4－01 | $x^{\prime}$ A 3－17 | XA15－E | XA 5 － 1 | xa 5－01 |
|  | 7－17 | XA 3－V | 1415－02 | XA 4－${ }^{\text {－}}$ | XA $3-18$ | XA15－U | XA 6－J？ | XA b－0， |
| J | ＜－18 | XA 3－07 | 1S1H－02 | XA 4－02 | XA 3－19 | J 2－1 | XA 6－35 | X $\mathrm{A}^{\text {5－}} 5$ |
| J | －19 | xA 3－08 | TB1C－01 | XA 5－A | XA 3－19 | XA14－23 | xA 3－Js | XA 7－U |
| J | ＞－20 |  | THIC－01 | XA 5－01 | XA 3－20 | XA15－11 | xA 6－09 | xA15－19 |
| J |  | xA 1－01 | TBIC－02 | XA 5－${ }^{\text {P }}$ | xA 3－21 | xals－N | XA 6－14 | XA15－$x$ |
| J | 3－1 | TB1a－31 | THIC－02 | XA 5－02 | XA 3－22 | J $2-\mathrm{V}$ | XA 5－15 | $x A 5-w$ |
| J | 3－A | J 3－C | TH10－01 | XA 7－A | XA 4－ | XA 4－F | xA 6－15 | xA 7－23 |
| J | 3－6 | J 3－0 | T310－01 | XA 7－01 | XA 4－${ }_{\text {－}}$ | TВ18－0？ | $x \times 1818$ | XA 5－E |
| J | 3－C | J 3－4 | TR10－02 | $\times \mathrm{A} 7-\mathrm{B}$ | $X A$－C | XA 3－C | XA 0－19 | XA 7－S |
| J | 3－0 | J 2－A | TB10－02 | XA $7-02$ | XA 4－C | XA 5－C | XA A 20 | XA15－22 |
| J | 3－0 | J 3－b | TA1t－01 | XA 9－A | XA 4－U | XAL6－F． | XA 6－7 ${ }^{\text {P }}$ | XA 5－1． |
| J | 3－6 | $\times$ A 7－17 | TUEEU1 | XA10－04 | KA 4－E | J 1－K | xA 6－23 | XA 7－8 |
| J | 3－H | $\times \mathrm{A}$ 7－J9 | TH1F－0？ | XA 9－B | XA 4－F | XA 4－A | XA 7－A | THLU－02 |
| J | s－K | $\times 4$ 1－08 | THIF－Cl | XAIL－ 4 | XA 4－F | TH18－01 | xA 7－A | XA A－A |
| J | 3－M | XA T－19 | TAIF－01 | xal2－x | XA 4－01 | TB18－31 | XA 7－B | TR1U－02 |
|  | 3－P | XA 7－ | TRIF－02 | XA11－8 | XA 4－02 | TH18－02 | XA 7－B | $\times \mathrm{A}$ 8－${ }^{\text {－}}$ |
|  | 3－S | XA 7－10 | TH1G－01 | XA13－${ }^{\text {a }}$ | XA 4－03 | $\mathrm{XAF}_{4} 3-03$ | XA 7－${ }^{\text {P }}$ | XA 5－c |
|  | 3－U | $\times$ ¢ $7-i) 7$ | TA16－01 | XA13－01 | XA 4－03 | $X_{\text {A }}$ 5－03 | XA 7－0 | XA 9－07 |
|  | 3－W | XA15－13 | TR1G－02 | XA13－${ }^{\text {－}}$ | XA 4－04 | $x_{A}$ 4－22 | XA 7－F | XA B－P |
| J | 3－Y | xA15－i） | 1ヵ16－02 | XA13－02 | XA 4－05 | J 1－v | XA T－F | XA 9－${ }^{\text {P }}$ |
|  | $3-2$ | $\times$ A15－07 | TH1H－01 | XA15－4 | XA 4－06 | XA 5－10 | XA $\mathbf{7 - H}$ | XA10－07 |

LOGIC ASSEMBLY AI（ WITHOUT T．K．G．）WIRE LIST

| FROM | TO | FROM | TO | FROM | TO | FROM | TO |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Cun－riv | CUV－PIV | c3y - P1 | 二ON－PIN | $\mathrm{CCN}-\mathrm{PIN}$ | CON－PIN | CUN－PIN | cov－${ }^{\text {dV }}$ |
| x A 7－J | XA14－H | XA H－14 |  | XALO－P | XA $7-\mathrm{C}$ | X A11－15 | x A12－16 |
| $\times \pm 7-2$ | XA $\mathrm{X}-73$ | $\times \mathrm{A}$（ $\mathrm{H}-25$ | $\times{ }^{1} 7-$ | XA10－R | ха 7 － 5 | XA1t－1t | $\times \mathrm{Al2-2}$ |
| XA 7－L | $\times$ ¢ $\mathrm{X}-15$ | XA H－15 | $x$ A $\mathrm{A}^{\text {－}}$ | xal 0－S | $\times$ ¢ $7-35$ | $\times$ A11－17 | ＊A12－E |
| $\times \mathrm{A} 7-\mathrm{M}$ | XA13－19 | XA 9－16 | x 11 c－12 | XA10－ | $\times A L ?-1$ | X A11－18 | $\times 412-10$ |
| $\times \mathrm{A} 7-\mathrm{v}$ | $X A G-X$ | XA 8－17 | XA 9－13 | 2A10－ 9 | X $A \rightarrow-\mathrm{D}$ | $\times$ A11－17 | $\times$＋12－08 |
| $\times \mathrm{A} 7-\mathrm{P}$ | $\times \mathrm{A}-$ | $\times 48-18$ | $x \triangle$ \＆－ | xalio－v | XA 7 － 33 | $\times$（11－2） | $\times$（12－05 |
| $\times$－7－ | $\times$ x $6-13$ | $x_{4} x_{4}$ ？－19 | XA S－AA | xal0－ | $\times \mathrm{Al3}-\mathrm{M}$ | $\times \mathrm{AlI}-21$ | ＋A12－19 |
| XA 7－S | $\times \wedge$－－－ | $\times 4$ R－20 | XA11－22 | xAIO－$x$ | XA 7－V | $\times$ A11－22 | $\times$（ G－70 |
| $\times$ A $7-1$ | J 3－$\mu$ | xA 8－71 | XA ¢－11 | XA1 0－Y | XA 7－39 | $\times$ A11－23 | $\times$－9－23 |
| $\times{ }^{\prime}$－7－J | $x$ A $0-05$ |  | X $111-$ | XA10－ 2 | XA $3-\mathrm{N}$ | $\times \mathrm{Al2-A}$ | $\times$－12－07 |
| $x \wedge 7-\vee$ | $\times$ A13－04 | $\times 4$ 9－7 ${ }^{14}$ | $x A 7-1$ | XALO－AA | XA 7－13 | xAl？－${ }^{\text {a }}$ | $\times \mathrm{A12-D}$ |
| $x$ A $7-x$ | $\times 413-10$ | XA 9－4 | THIE－CI | XA10－01 | X A13－34 | XAL2－${ }^{\text {P }}$ | XA11－${ }^{\text {A }}$ |
| $\times$ A $7-$ | $\times \triangle$－ | $x 498$ | $x \rightarrow 10-4$ | xalo－0？ | XA12－32 | $\times \mathrm{Al2-C}$ | （A11－${ }^{\text {a }}$ |
| $\times{ }^{\times 17} 7$ | $\times$ A 8－04 | X4 9－3 | T3 1t－c2 | $\times 110-03$ | $x$ x ${ }^{\text {x 3－23 }}$ | $\times 412-0$ | $\times \mathrm{A12-a}$ |
| $\times A$ 7－AA | ¢ 2－35 | X4 9－9 | $\times \mathrm{A} 1 \mathrm{C}^{-1}$ | $\times 110-04$ | x A13 -31 | $x$ Al2－0 | $\times$ x12－U |
| $\times$－$\quad 1-01$ | T B bu－${ }^{\text {a }}$ | X4 9－ | XA10－P | $\times \mathrm{Al} 0-04$ | TBLE－31 | $\times \mathrm{Al2-5}$ | $\times$ A11－17 |
| $\times$－7－01 | xA y－ul | X4 9－） | $x A_{1-1}$ | XA10－05 | X4 7－17 | XAL2－F | $\times \mathrm{All-08}$ |
| $\times 4!-02$ | 「810－02 | $X A$ 9－E | XA 8－D | $\times 410-06$ | $\times 4$ 9－4 | XALI－H | $\times \mathrm{AlO}-\mathrm{H}$ |
| $\times 47-0$ ？ | $x A 8-02$ | $X A$ 9－E | XAll－E | kA1 0－06 | XA13－E | $\times \mathrm{Al2-H}$ | $\times 113-2$ |
| $\times \mathrm{A} 7-03$ | $\times$ A14－05 | X4 9－ | $x_{A}$ 9－t | XA1 0－07 | XA 7－H | XAl2－J | $\times 410-J$ |
| $\times \mathrm{A} 7-04$ | $\times \mathrm{A}$－ | XA 9－$F$ | XA11－F | KA1 0－07 | XAl1－P | $\times$ Al2－ | $\times$（13－16 |
| XA 7－05 | $\times$ A11－07 | $X 4$ \％H | XA10－C | $\times \mathrm{ALO} 0 \mathrm{OB}$ | XA 7－37 | $\times$ A12－＜ | XALI－S |
| ＜A l－0a | $\times$ Al4－N | $\times 49$ | XA $1 \mathrm{C}-22$ | $\times 410-09$ | XA13－0 | XA12－ | $\times \mathrm{A11-05}$ |
| $\times A 7-1) 7$ | 3－U | $x$ X 4 －K | $x \pm 1 C-1 C$ | xal 0－09 | $\times 4$－ | XAl2－ 4 | $\times$（11－0＇4 |
| $\times$－ $7-98$ | J 3－＜ | $x 492$ | $x A 10-21$ | KA1 0－10 | $\times 4 \rightarrow$－$\times$ | $\times \mathrm{Al2-N}$ | $\times \mathrm{A} 10-\mathrm{V}$ |
| $\times$－ $7-09$ | J 3－4 | $x 49-9$ | XAIO－C | K410－11 |  | $x$ Al2－y | XA13－15 |
| $\times$ A 7－10 | $J$ 3－5 | XA 90 | XA1C－ 2 | xA1 0－12 | XA $x^{4-15}$ | XA12－p | $\times \mathrm{Al1-2}$ |
| $\times \wedge 7-11$ | 5 2－02 | XA 9－${ }^{\text {¢ }}$ | XA 7－${ }_{\text {F }}$ | KA10－1？ | XA13－36 | XA12－R | xall－ C |
| （A 7－12 | $\times$ A13－13 | $\times 49$ | XALC－16 | xA10－13 | xall－13 | XA12－ | $\times \mathrm{A11-}$ |
| $\times$（ $1-13$ | $\times$ Ali－ H | $x \wedge 9$ | XA1C－R | Ma10－14 | XA13－N | XA12－ | $\times$ ALO－${ }^{\text {¢ }}$ |
| （A 7－14 | $x A 8-C$ | $\times 4$ | XA－ $\mathrm{Cb}^{\text {¢ }}$ | xal 0－15 | X413－14 | XAl2－ | $\times$ A13－22 |
| $\times$－7－14 | $\times$－ $\mathrm{x}-03$ | $\times 4$ 9－ | XA11－${ }^{\text {P }}$ | XA1 0－16 | XA $7-\mathrm{R}$ | XA12－J | XA12－0 |
| $\times$－7－15 | $\times 413-07$ | $\times 4$ 9－6 | XA 8－C7 | XA1 0－1 ${ }^{\text {P }}$ | XA $9-15$ | $\times$ A12－ | $\times$ X11－14 |
| $\times$－7－16 | $\times 45-07$ | XA 9－u | XA11－1 | xal 0－19 | XA $7-17$ | $\times \mathrm{Al2}=$ | $\times$ A13－20 |
| $\times \mathrm{x}$－7－17 | J 3－E | $\times 4$ 9－ | $\times 11 \mathrm{C}$ | $\times 410-19$ | XA 9 －21 | $\times$ Al2－ | $\times$ A12－13 |
| $\times \mathrm{CA} 7-1 \mathrm{C}$ | $J$ 3－03 | XA 9－ | $\times 480$ | xA1 0－20 | xAl 2－2 | $\times \mathrm{Al2-}$ | IB1F－01 |
| $\times$－7－19 | J 3－4 | X4 9 | XA B－Cs | KA1 0－21 |  | $\times \mathrm{Al2-r}$ | xall－v |
| XA 7－70 | $X A R-J$ | $x$ ¢ 2 | XA11－ | $\times 110-2 ?$ | X4 7－」 | $\times \mathrm{Al2-}$－ | xA11－16 |
| $\times$－ $7-21$ | $\times$ A13－C | $X A 9$ | xa 8－12 | XA10－21 | XA1 2－23 | $\times A 12-4 A$ | xall－＊ |
| $\times$ ¢ 7－2．2 | $\times 413-17$ | $\times 4$ 9－1 | X413－C4 | XAII－${ }_{\text {a }}$ | T $\mathrm{Bl} \mathrm{F}-\mathrm{j} 1$ | $\mathrm{xA12-31}$ | $\times$－12－06 |
| $x$（ 1－23 | $x \times t=15$ | XA 9－AA | XA 8－15 | XAII－${ }^{\text {a }}$ | $\times \mathrm{Al2-37}$ | $\times \mathrm{Al2-3} 2$ | $\times \mathrm{A10-02}$ |
|  | $\times 47-1$ | XA－ 9 Cl | XA－ CS | XA1 1 － $\mathrm{A}_{1}$ | T $\mathrm{AlF-32}$ | $\mathrm{xA12-32}$ | $\times$ A13－AA |
| XA H $=\mathrm{H}$ | XA 7－R | XA 9－0 | XA11－C1 | XAIL－${ }^{\text {P }}$ | $\times \mathrm{Al2-H}$ | x A12－3 | $\times$ A13－09 |
| XAP－C | $\times 4$ 7－14 | $x 4$ 9－02 | XA $10-\mathrm{E}$ | XA11－C | XAl2－R | $x$ Al？－34 | $\times 48-11$ |
| $X A P=D$ | $\times 49-1$ | XA 9－03 | $X A 1 C-1$ | XAIL－0 | XAL $2-\mathrm{C}$ | $\times \mathrm{A12-35}$ | $\times$ A11－20 |
| XAR－E | $\times 49-F$ | XA 9－04 | $\times 410-m$ | XAIL－E | XA 7－E | $\times \mathrm{A12-J3}$ | $\times \mathrm{Al2-01}$ |
| $X A R-E$ | XA 9－12 | XA 9－C5 | XA 10 | XA11－F | XA 7－F | $\times$ A12－36 | x A12－13 |
| $X A R=H$ | $x A-23$ | XA 9－03 | XA1C－ | XAIL－${ }^{\text {d }}$ | XA12－V | X A12－37 | $\times$ A11－${ }^{\text {a }}$ |
| $x A P-J$ | $\times \mathrm{A} 7-20$ | xA－07 | $X A 7-0$ | XAII－J | XA12－19 | ＊A12－07 | XA12－${ }^{\text {a }}$ |
| XAR－J |  | X4 9－07 | XAIC－CE | XAIL－K | XA12－5 | $\times \mathrm{A12-08}$ | xA11－19 |
| $x A 8=k$ | $\times$ ¢ $\mathrm{H}-13$ | X4 9－08 | $X A L C-Y$ | XALI－L | $x$ A12－2？ | $\times$ A12－39 | $\times$ A11－02 |
| xA $8-k$ | $\times \mathrm{Al4-S}$ |  | $x_{A A} \quad 8-1 \mathrm{C}$ | XA11－M | XAL $2-A A$ | X A12－17 | X A11－18 |
| xAq－L | $\times$－7－04 | XA 9－10 | XA 10－17 | XALI－v | XAL2－Y | $\times$ A12－11 | （A11－03 |
| YA B－Y | $\times$ A10－06 | XA 9－11 | XA 8－21 | XALI－p | XA1 J－37 | $\times \mathrm{Al2-17}$ ？ | XA11－06 |
| $\times \mathrm{A}:-\mathrm{N}$ | xall－ Y | X4 9－12 | $X A 8-F$ | XA1 1－ P |  | $\times 412-13$ | $\times$ A12－06 |
| XA B － P | $x A 7-t$ | XA 9－12 | XA11－12 | XAIL－R | XA12－P | X A 12－13 | x A12－ x |
| KA $8=R$ | $x A x-J$ | X4 9－13 | $x_{A} \quad 8-17$ | XAIL－S | XAI2－K | XA12－14 | XA13－ x |
| KA M－S | $\times$ A 8－18 | $x 49-14$ | XALC－F | xall－ | XA 7－ 1 | XA17－15 | XA13－21 |
| x $A \leq-T$ | $\times$ A11－13 | X4－ 15 | $X A \subset C-K$ | XAIL－U | $X A 7-U$ | X A12－16 | XA11－15 |
| ＊AB－U | $\times \mathrm{A}$－ P | xA 9－16 | $X A 1 C-D$ | XAIL－ | XA12－17 | X A12－17 | $\times$ All－$V$ |
|  | $\times$－${ }^{\text {A }}$－ 15 | x4 9－17 | $\times{ }^{\text {a } 10-18}$ | XALI－W | XA 9－22 | $\times 412-18$ | xall－J |
| XA 9 － | $\times A$ 9－${ }^{+}$ | X4 9－18 | XA10－AA | XAIL－$x$ | $x$ P $7-X$ | X 412－17 | XA11－21 |
| XA $4=$ | $\times$＾9－22 | XA 9－19 | XA 10－C5 | XAL 1 －$Y$ | $X \mathrm{XA}-\mathrm{N}$ | $\times$ A12－2） | XALO－20 |
| $\times$ A 9 － | $\times \mathrm{A}$－ U | $X^{\prime} 49-20$ | $\times 110-11$ | $x x^{\prime} 1-2$ | XA13－35 | $\times$ A12－23 | $\times \mathrm{Al3-18}$ |
| $\times \mathrm{A}=2$ | $\times$ All－AA | $\mathrm{XA}_{4}+21$ | $x A_{1} \mathrm{c}-19$ | XAII－AA | XA 9－2 | xA12－21 | XA11－14 |
| $\times A \leq-A 4$ | x AIt－11 | $x 4$ 9－22 | $\mathrm{XA} \mathrm{H}_{4} \mathrm{~B}-\mathrm{y}$ | XAIL－01 | XA 7－31 | x A12－22 | $\times$ A11－ |
| $\times 49-01$ | $\times$－ 7 －01 | $\times 4$ 9－23 | XA \％-H | XA11－02 | XA12－37 | XA12－23 | XA10－23 |
| $\times$ ¢ 9－i） | $\times$－ $7-\mathrm{C2}$ | $x 40-23$ | XA11－23 | XAII－03 | xal2－11 | $\times$ A12－23 | XA13－ |
| X $A$ 3－03 | XA 7－14 | $\times \mathrm{A} 10-\mathrm{A}$ | $\times 4$ \％${ }^{1}$ | XA11－04 | XAL2－M | $\times$ A13－A | TBIG－01 |
| $\times$ ¢ 8－04 | $\times$－7－ 2 | KA10－${ }^{\text {a }}$ | $X_{4}$ \％－${ }_{\text {B }}$ | XA11－05 | XA12－L | $\times$ A13－A | KAl4－A |
| $x$ A 8 － 14 | XA R－14 | KA 10－ | XA 9－H | XAll -08 | XA12－12 | $\times \mathrm{Al3-}{ }^{\text {P }}$ | TBLG－02 |
| $\times \mathrm{A}$－ $\mathrm{C}_{\text {－US }}$ | $\times \wedge$－ 01 | XA10－0 | $x_{4}$ 9－16 | Xall－07 | XA 7－35 | $\times \mathrm{Al3-B}$ | $\times$－ $14-8$ |
| $\times 4$ 9－96 | $\times \mathrm{A} 9-1$ | $\times 410-\%$ | $\mathrm{XA}_{4} 9 \mathrm{Cl}$ | XA11－03 | XAL2－F | $\times$ A13－C | XA T－21 |
| X $\triangle$ y -07 | $\times$ ¢ 9－U | $\times 410 \mathrm{~F}$ | x ${ }_{4}$－ 14 | XALI -09 | XA 9－37 | XA13－D | $\times \mathrm{AlO-08}$ |
|  | $\times \mathrm{A} 9-\mathrm{x}$ | $\times 110-4$ | XA12－ H | XAL $1-10$ | XA1 J－13 | $\times \mathrm{Al3-E}$ | $\times$ A 10－06 |
| $\times \mathrm{A}$－ OH | $\times 411-09$ | KA 10－3 | x $\mathrm{A}_{12-\mathrm{J}}$ | $x$ A11－10 | XAL3－F | $\times$ A13－+ | XA11－10 |
| $\times A \leq-1 ?$ | K A 9－09 | $\times 100 \mathrm{~K}$ | XA 9－15 | xall－LI | XA 3－AA | $\times$ A13－H | $\times$（ 7－13 |
| $\times$ A 3－11 | $\times$ A12－04 | $\times 1.10$ | $\mathrm{XAA}_{4} 9 \mathrm{C5}$ | xall－1？ | $\times 47-12$ | $\times \mathrm{Al3-M}$ | $\times \mathrm{AlO}-1$ |
| X $A$ R－12 | $\times$－9－Y | XA10－M | $\mathrm{XAA}_{4}$ ¢－ $\mathrm{CL}_{4}$ | xA11－13 |  | $\times$ A13－${ }^{\text {－}}$ | XA10－14 |
| $\times$ A $8-1.3$ | $\times$ ¢ ${ }^{\text {¢ }}$ | $\times 410-\mathrm{V}$ | XA12－N | XA11－14 | xa12－21 | $\times$ A13－P | KA12－ H |

LOGIC ASSEMBLY A（ WITHOUT T．I．G．）WIRE LIST

| FROM | TO | FROM | TO | FROM | TO | FROM | TO |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| con－pin | cov－piv | CJV－PIN | CON－PIN | CON－PIN | CON－PIN | CON－PIN | COV－P 1 |
| x413－${ }^{\text {¢ }}$ | x A12－23 | X415－C3 | $\times 4$ 4－2C |  |  |  |  |
| XA13－X | XA12－14 | XA15－03 | X 116 |  |  |  |  |
| X A13－AA | xA12－02 | XA 15－04 | XA 3－${ }^{\text {a }}$ |  |  |  |  |
| $\times$ A13－01 | 18ig－01 | X415－C5 | XA 16－16 |  |  |  |  |
| $\times$ Al3－01 | XA14－01 | XA15－67 | J 3－ |  |  |  |  |
| $\times$ A13－02 | TB1G－02 | X415－C8 | J 3－ |  |  |  |  |
| $\times$ A13－02 | $\times \mathrm{Al4-02}$ | X415－09 | x 1－14 |  |  |  |  |
| XA13－03 | XA11－P | XA15－10 | 5 1－NO |  |  |  |  |
| $\times 413-04$ | xA 9－$Z$ | XA 15－11 | XA 3－2C |  |  |  |  |
| XA13－05 | XA11－Z | X415－12 | XA 4－22 |  |  |  |  |
| $\times$ A13－26 | $\times \mathrm{AlO-12}$ | X 4 15－12 | xal $16-23$ |  |  |  |  |
| $\times 413-07$ | $\times$ A 7－15 | X 4 15－13 | 」 3－ |  |  |  |  |
| $\times$ A13－08 |  | XA15－14 | xalb 2 |  |  |  |  |
| $\times$ A13－09 | $\times 117-03$ | XA 15－15 | XA14 ${ }^{\text {x }}$ |  |  |  |  |
| $\times$（13－17 | $x$ A 7－x | XA 15－16 | $x$－5－1 1 |  |  |  |  |
| $\times$－13－13 | $\times 47-12$ | XA15－16 | X $\mathrm{Al}_{15}^{5-1}$ |  |  |  |  |
| X413－14 | $\times \mathrm{AlO-15}$ ． | $\times \mathrm{x}$ 15－17 | x 4 －12 |  |  |  |  |
| X A13－15 | x A12－${ }^{\text {¢ }}$ | X415－18 | X 14 － Cb |  |  |  |  |
| x A13－16 | $\times$ A12－J | XA15－19 |  |  |  |  |  |
| $\times$ A13－17 | XA 7－22 | XA15－20 | x 4 －ce |  |  |  |  |
| $\times \mathrm{A13-18}$ | $\times 1.20$ | XA15－21 | X $\mathrm{H}_{14-}$ |  |  |  |  |
| $\times$（13－19 | $\times \mathrm{A} 7-\mathrm{M}$ | $\times \mathrm{X}$ 15－21 | $\times 1.6$ |  |  |  |  |
| X A13－20 | $\times \mathrm{Al2-}$ | x $\times 15-22$ | $x A 6-2 c$ |  |  |  |  |
| xA13－21 | XA12－15 | X 15－23 | XA 14－15 |  |  |  |  |
| $\times$ 113－22 | $\times$ A12－ 5 | X415－23 | XA16－19 |  |  |  |  |
| x413－73 | $\times \mathrm{ALO} 03$ | xalt A |  |  |  |  |  |
| $\times$ A14－A | $\times$ A13－${ }^{\text {a }}$ | XA16－8 | XA15－8 |  |  |  |  |
| $\times \mathrm{Al4-8}$ | $\times$ A13－ | x416－6 | XA14－C8 |  |  |  |  |
| $\times \mathrm{Al4-} \mathrm{D}$ | XA 1－0 | XA 16－${ }^{\text {d }}$ | XA15－R |  |  |  |  |
| XA14－ H | $\times \mathrm{A}{ }^{\text {P－J }}$ | $\times 416-E$ | XA 15－1t |  |  |  |  |
| XA14－K | $\times \mathrm{Al5}$－ | X416－f | $x x^{4}$ 4－0 |  |  |  |  |
| XA14－S | $\times 48$－ | XAIGO H | XA15－0 |  |  |  |  |
| XA14－ | $\times \mathrm{x} 3-\mathrm{F}$ | XAIto K | $J$ 2－ H |  |  |  |  |
| XA14－＊ | $\times$ ¢ 7－06 | x 1 $^{16-N}$ | XA15－21 |  |  |  |  |
| xA14－＊ | $\times$ A15－21 | XA16－P | XA15－C3 |  |  |  |  |
| xA14－x | X A15－15 | XA16－${ }^{\text {P }}$ | J 2－R |  |  |  |  |
| xA14－2 | $\times$ A15－20 | XA 16－T | 」 2－N |  |  |  |  |
| $\times$（14－01 | XA13－01 | XA16－W | J 2－${ }^{\text {－}}$ |  |  |  |  |
| $\times$ A14－02 | $\times$ A13－02 | X $416-x$ | XA15－ 1 |  |  |  |  |
| $\times$ A14－05 | XA 7－03 | XA16－ Y | $x A^{\text {a }}$ 3－ K |  |  |  |  |
| x A14－06 | X4 5－14 | $x \triangle 16-2$ | XA L5－14 |  |  |  |  |
| X A14－06 | X A15－19 | xaltras | J 2－J |  |  |  |  |
| X A14－08 | $\times \mathrm{A} 3-\mathrm{D}$ | XA 16－01 | XA15－C1 |  |  |  |  |
| $\times \mathrm{Al4-08}$ | $\times$ A16－ 6 | xA16－02 | XA15－C2 |  |  |  |  |
| X A14－09 | $\times \mathrm{Al5-Y}$ | XA16－03 | XA15－N |  |  |  |  |
| X A14－10 | $\times \mathrm{Al5-}{ }^{\text {－}}$ | X416－04 | XA15－Y |  |  |  |  |
| X A14－14 | $\times 415-1$ | X ${ }^{16-05}$ | XA 3－16 |  |  |  |  |
| X A14－15 | XA15－－ | xa 16－C6 | KA 3－E |  |  |  |  |
| X A14－19 | XA 1－T | XA16－c7 | XA 14－2C |  |  |  |  |
| XA14－19 | X415－23 | XA 16－08 | XA 4－16 |  |  |  |  |
| XA14－20 | XA16－07 | XA16－10 | XA15－F |  |  |  |  |
| $\times$ A14－23 | XA 3－19 | xalb－ 11 | J 2－L |  |  |  |  |
| xAlb－A | TAIH－O1 | XA16－12 | 」 2－k |  |  |  |  |
| $\times \mathrm{Al5-A}$ | $\times$ A16－A | X416－13 | J 2－F |  |  |  |  |
| KA15－B | T81H－02 | XA 16－14 | XA 3－15 |  |  |  |  |
| xa15－8 | $\times \mathrm{Al6-B}$ | xalo－15 | XA15－H |  |  |  |  |
| xA15－ C | XA 4－10 | XA16－18 | XA15－c5 |  |  |  |  |
| XA15－${ }^{\text {d }}$ | $\times$ Al6－ H | xals－17 | J 2－P |  |  |  |  |
| XA15－E | XA 3－17 | XA16－18 | J 2－M |  |  |  |  |
| XAlb－F | XA 4－18 | X416－19 | XA15－23 |  |  |  |  |
| XA15－F | $\times$ A16－10 | XA 16－20 | $\times \mathrm{A} 14-2$ |  |  |  |  |
| （A15－ H | X A 3－14 | XA 16－21 | XA $4-23$ |  |  |  |  |
| （Al5－$\mu$ | x A16－15 | X $\times 16022$ | J 2－${ }^{\text {a }}$ |  |  |  |  |
| XA15－K | $\times 114-\mathrm{R}$ | $\times 416-23$ | XA15－12 |  |  |  |  |
| XA15－l | X A14－14 |  |  |  |  |  |  |
| xA15－1 | XA1t－ X |  |  |  |  |  |  |
| XA15－4 | $\mathrm{XA} 3-\mathrm{J}$ |  |  |  |  |  |  |
| （A15－N | $\times$ A 3－21 |  |  |  |  |  |  |
| ＊ALS－N | XA16－03 |  |  |  |  |  |  |
| X A15－K | xAlts－${ }^{\text {d }}$ |  |  |  |  |  |  |
| －A15－ | XA14－10 |  |  |  |  |  |  |
| －A15－U | xA 3－18 |  |  |  |  |  |  |
| $\times$ A15－＊ | ＊A14－15 |  |  |  |  |  |  |
| xal5－x | xA 6－14 |  |  |  |  |  |  |
| －A15－ Y | $\times$ A14－09 |  |  |  |  |  |  |
| －A15－ Y | $\times$ A16－04 |  |  |  |  |  |  |
| $\times$ A15－0 | TB1H－01 |  |  |  |  |  |  |
| $\times$ A13－01 | XA16－01 |  |  |  |  |  |  |
| $\times \mathrm{AL5-02}$ | TB1H－02 |  |  |  |  |  |  |
| x415－02 | $\times$ A16－02 |  |  |  |  |  |  |

TM 7440－219－15－WL－1－（3）
Figure 8－24（3）．Logic Assembly A1（without TIG），interconnection chart（part 3 of 3）．

LOGIC ASSEMBLY AI（ WITH T．I．G．）WIRE LIST

|  | FROM | TO | FROM | TO | FROM | TO | FROM | TO |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | ON－PIN | CON－PIN | CON－PIN | CON－PIN | CUN－PIN | CON－PIN | CUN－PIN | CON－PIN |
|  | 1 | ［日 2－7B | 」 3－ | XA15－13 | TB 2－58 | xa 3－01 | $x \pm 2-y$ | XA 6－ 7 |
|  | 1 | J 1－AA | J 3－Y | XA15－08 | TB 2－78 | E 1 | $x$（ 2 － | J 4－K |
|  | $?$ | J 2－4A | J 3－L | XA15－01 | TB 3－18 | T8 1－01 | $x$ X $2-x$ | XA 5－Y |
|  | 3 | J 3－AA | J 3－AA | E 3 | TB 3－28 | 18 1－02 | XA $2-Y$ | $\times 4$ 5－1 |
|  | 4 | $J$ 4－AA | J 3－01 | J 2－01 | TB1A－01 | ＋3－A | XA 7－2 | XA 5－E |
|  | 1－A | XA 2－13 | J 3－01 | J 3－05 | 181A－01 | $\times 1$ 1－A | XA $2-A A$ | XA 5－07 |
|  | 1－8 | J 4－P | J 3－03 | x 4 7－18 | TBIA－02 | $\times$ 1－8 | xa 2－ul | J 4－02 |
|  | 1－L | XA 4－21 | 」 3－05 | J 3－01 | TB1A－02 | x ${ }_{\text {A }} 1-02$ | xA $2-01$ | J 4－03 |
|  | $1-\mathrm{N}$ | X $\times 4$－ 14 | J 3－05 | 」 3－07 | TH18－01 | XA 4－f | XA 2－01 | $\times$－ $3-4$ |
|  | 1－R | XA 4－E | 」 3－07 | J 3－05 | 1818－01 | XA 4－01 | XA $2-02$ | J $4-07$ |
|  | l－T | XA $4-11$ | J 3－07 | 」 3－09 | 1818－02 | XA 4－B | XA 2－02 | $x$－ 4 － 6 |
|  | $1-\mathrm{V}$ | XA $4-05$ | J 3－09 | 」 3－07 | T818－02 | XA 4－02 | X ${ }^{\text {A }} 2-03$ | XA 3－03 |
|  | 1－X | $x$ ¢ 4－13 | J 3－09 | J 3－11 | rilc－01 | XA 5－A | XA $2-04$ | $\times{ }^{\times 1} 4-0$ |
|  | 1－2 | X4 4－09 | J 3－11 | J 3－09 | T8iC－01 | XA 5－01 | XA 2－05 | XA14－06 |
|  | 1－AA | E 1 | 」 3－11 | J 3－13 | 1BIC－02 | $X A$ S－B | XA 2－06 | 」 4－05 |
|  | 1－01 | XA 5－U | J 3－13 | J 3－11 | T81C－02 | XA 5－02 | XA $2-36$ | xals－0 |
|  | 1－03 | XA 5－V | J 3－13 | J 3－15 | TA10－02 | XA 7－a |  | XA14－10 |
|  | 1－05 | $X A 5-X$ | 」 3－15 | J 3－13 | TB10－01 | XA 7－01 | XXA 2－13 | J 1－A |
|  | 1－07 | XA 5－20 | J 3－15 | J 3－17 | TB1u－02 | XA 7－ 8 | XA $2-14$ | 」 4－04 |
|  | 1－09 | XA 5－0 | 」 3－17 | J 3－15 | 1810－02 |  | XA 2－15 | XA 8－15 |
|  | 1－11 | XA 5－F | J 3－17 | J 3－19 | TSIE－02 | XA 9－4 | XA $2-16$ | $\times 4$ 6－＊ |
|  | 1－13 | $\times 4$ 5－H | J 3－19 | J 3－17 | T815－01 | XA10－04 | XA $2-17$ | XA 6－05 |
|  | 1－15 | XA 5－J | J 3－19 | 」 3－21 | TBIE－02 | XA 9－${ }^{\text {d }}$ | XA $2-18$ | J 4－J |
|  | 1－17 | XA 5－12 | 」 3－21 | J 3－19 | THif－0］ | XAII－A | XA 2－19 | $\times 1$ 6－X |
|  | 1－19 | XA 4－J7 | J 3－22 | $J$ 2－A | TAlf－01 | XA12－ X | $\times 4$ 2－20 | $\times \mathrm{A} 5-1$ |
|  | 1－21 | XA 4－17 | J 3－22 | XA 1－01 | TBIF－02 | XAII－ 0 | XA $2-21$ | $X A 5-K$ |
|  | 1－23 | XA 4－19 | J 4－A | XA 2－${ }^{\text {－}}$ | THig－01 | XA13－A | xA 2－22 | x A $5-21$ |
|  | 2－A | J 3－22 | J 4－8 | XA 2－$M$ | TBIG－01 | XA13－01 | XA $\geq-23$ | XA 5－2 |
|  | 2－A | $\checkmark$ 3－${ }^{\text {J }}$ | J 4－C | $\checkmark$ 2－C | T81G－02 | XAL3－${ }^{\text {P }}$ | XA 3－A | тi $2-53$ |
|  | 2－C | J 4－C | J $4-C$ | $\times \mathrm{XA}-\mathrm{C}$ | TB16－02 | XA13－02 | XA 3－A | XA 2－01 |
|  | 2－C | 」 $3-04$ | J 4－C | 10 2－18 | TBIH－01 | XALS－A | XA $3-\mathrm{C}$ | $\times \mathrm{A}$ 1－C |
|  | 2－F | xA15－13 | J 4－0 | XA 2－P | rolh－01 | XA15－01 | KA 3－C | XA $2-\mathrm{C}$ |
|  | ？－H | XA1G－K | J $4-E$ | XA $2-N$ | Tilri－02 | XA15－B | XA 3－C | XA 4－C |
|  | 2－J | XALS－AA | J $4-F$ | XA $2-\mathrm{R}$ | TB1H－02 | XA15－02 | XA 3－D | XA14－U8 |
|  | 2－k | XA15－12 | J $4-\mathrm{H}$ | XA 2－S | 181J－01 | S 1－C | XA 3－E | XA16－06 |
|  | 2－1 | XA1S－11 | J $4-\mathrm{J}$ | XA 2－18 | T81J－01 | $5 \quad 2-03$ | $\times$ A 3－F | J 2－U |
|  | 2－m | XA1S－18 | J $4-K$ | X $\mathrm{XA}^{2-1}$ | TB1J－02 | 5 2－01 | $\mathrm{XA} 3-F$ | XA14－V |
|  | 2－N | XA1S－ 1 | J $4=\mathrm{L}$ | XA 1－06 | XA 1－${ }_{\text {－}}$ | T81A－01 | KA 3－H | XA15－04 |
|  | ？－P | XALS－17 | $J$－${ }^{-1}$ l | XA 1－05 | XA 1－A | J 2－01 | XA 3－J | XA15－M |
|  | $2-R$ | XA16－R | J 4－p | J 1－B | XA 1－${ }^{\text {P }}$ | J 2－02 | XA 3－K | XA16－Y |
|  | 2－T | XA 3－19 | d $4-A A$ | E 4 | XA 1－B | 1 $614-02$ | XA 3－R | J 2－11 |
|  | 2－U | XA 3－F | J 4－01 | XA $2-1$ | $\times \mathrm{X}$ 1－B | XA 2－B | XA 3－S | J $2-06$ |
|  | 2－V | XA 3－22 | J $4-02$ | $\times$ X 2－01 | XA 1－C | 3 4－C | $\times A 3-1$ | J 2－09 |
|  | 2－ | XA15－${ }^{\text {W }}$ | J 4－03 | XA 2－01 | XA 1－C | To 2－18 | XA 3－U | J $2-16$ |
|  | 2－$x$ | XA16－22 | J 4－03 | J 4－09 | $\times \mathrm{A} 1-\mathrm{C}$ | XA 3－C | $\times 4$ 3－V | J 2－17 |
|  | 2－AA | E 2 | J 4－04 | XA 2－14 | XA 1－${ }^{\text {d }}$ | xa14－${ }^{\text {（ }}$ | $\times 4$ 3－w | J $2-12$ |
|  | 2－01 | J 3－01 | J 4－05 | XA 2－06 | XA 1－ 1 | XA14－19 | XA 3－X | J 2－20 |
|  | 2－01 | XA 1－A | J 4－06 | XA 2－${ }^{\text {－}}$ | XA 1－T | XA 2－0 | $X A 3-Y$ | J 2－15 |
|  | 2－02 | $\times \mathrm{A} 1-8$ | J 4－07 | XA 2－02 | XA 1－01 | J 3－2－2 | XA 3－01 | 」 2－14 |
|  | 2－04 | J 2－C | J 4－07 | J 4－08 | XA 1－01 | J 3－4 | XA 3－01 | TH 2－58 |
|  | 2－06 | $\times 13-5$ | J 4－08 | J 4－07 | XA 1－01 | XA 2－A | XA 3－03 | XA 1－03 |
|  | 2－07 | $\times{ }^{\times 4} 3-05$ | J 4－09 | J 4－03 | $\times$ x 1－02 | Th1A－02 | $\times 4$ 3－03 | XA 2－03 |
| J | 2－08 | $\times$ X 3－04 | J 4－09 | J 4－11 | $\times$ X 1－03 | T8 2－2． | $\times 4$ 3－03 | XA 4－03 |
|  | 2－09 | XA 3－ 1 | J 4－10 | XA 1－10 | XA 1－03 | XA 3－03 | $\times$ X 3－04 | J 2－08 |
|  | 2－10 | $\times$ X 3－09 | J $4-11$ | J 4－09 | XA $1-05$ | J． 4 －L | XA 3－05 | 」 2－07 |
|  | 2－11 | XA 3－R | J 4－11 | J 4－15 | XA 1－06 | J＊4－L | $\times$ X 3－06 | J $2-11$ |
|  | 2－12 | $\times \mathrm{A} 3-W$ | J 4－12 | J 4－13 | $X^{\times} \times 1-08$ | T8 2－48 | $\times \mathrm{xa} 3-07$ | J 2－18 |
| $J$ | 2－13 | $\times \mathrm{x} 3-06$ | J 4－13 | J 2－14 | $\times$ X 1－09 | T8 2－4B | $\times 1$ 3－08 | J 2－19 |
| $J$ | 2－14 | XA 3－01 | J 4－13 | J 4－12 | $\mathrm{XA}^{\text {A }} 1-10$ | J 4－10 | XA 3－09 | J $2-10$ |
| 」 | 2－14 | J 4－13 | J 4－14 | xA 1－14 | XA $1-10$ | TH 2－38 | $\times$ X 3－14 | XA15－${ }^{\text {－}}$ |
| $J$ | 2－15 | XA 3－Y | J 4－15 | J 4－11 | $\times{ }^{\times} \times 1-14$ | J 4－14 | XA 3－15 | XA16－14 |
| J | 2－16 | $x A 3-U$ | 5 1－C | T8！J－01 | XA 1－14 | XA15－09 | $\times \mathrm{xa} 3-16$ | XA16－05 |
| $J$ | 2－17 | $\times$ X 3－V | S $1-\mathrm{NO}$ | XA15－10 | $\times$－ $2-A$ | J 4－A | $\times$ ¢ $3-17$ | XA15－ |
| $J$ | 2－18 | $\times$ X 3－07 | 5 2－01 | S 2－06 | $X{ }^{+} \times 2-A$ | J 4－01 | $\times 4$ 3－18 | XA15－U |
| $J$ | 2－19 | $\times$ x 3－08 | 5 2－01 | TA！J－02 | XA 2－$A$ | X4 1－01 | X4 3－19 | 」 2－T |
| $J$ | 2－20 | $\times$ ¢ 3－x | \＄2－02 | XA 7－11 | XA 2－${ }^{\text {B }}$ | J 4－06 | KA 3－19 | XA14－23 |
| J | 3－4 | J 3－C | S 2－03 | TR1J－01 | XA 2－${ }^{\text {－}}$ | XA 1－B | $x$ x 3－20 | XA15－11 |
| J | 3－A | T BIA －01 | S 2－03 | 5 2－04 | XA $2-\mathrm{C}$ |  | XA 3－21 | XA15－N |
| J | 3－A | $\times 4$ 1－01 | $5 \quad 2-04$ | $52-03$ | XA 2－0 | XA 1－T | XA 3－22 | J 2－v |
| J | 3－8 | J 3－0 | $5 \quad 2-05$ | XA 7－AA | $\times$－2－E | XA 5－14 | XA 4－4 | XA 4－F |
| J | 3－C | 」 3－A | 5 2－06 | 5 2－01 | $>^{x A} 2-F$ | $\times 415-16$ | XA 4－3 | XA 2－02 |
| $J$ | 3－0 | J．？－ 4 | T⿴ 1－01 | Јв 3－18 | XA．2－H | X $x_{4} 4-06$ | $\times 4$ 4－ | TBLB－02 |
| $J$ | 3－0 | J 3－B | Y⿴囗 $1-02$ | f8 3－2B | $X^{\prime} A 2-K$ | XA 4－18 | $\times 44-\mathrm{C}$ | XA 3－C |
| ， | 3－E | $\times \mathrm{A} 7-17$ | TE 2－18 | J 4－C | XA 2－${ }^{(1)}$ | J 4－b | $\times 44-\mathrm{C}$ | $\times \mathrm{A} 5-\mathrm{C}$ |
| $J$ | 3－H | $\times$－ $7-09$ | TB 2－18 | KA 1－C | XA 2－${ }^{\text {N }}$ | J $4-E$ | X $\times 4-0$ | $\times \mathrm{A} 2-04$ |
| $J$ | 3－K | $\times \mathrm{XA} 7-08$ | TB 2－2B | XA 1－03 | XA 2－P | J 4－0 | XA 4－ | $\times \mathrm{Al6}-1$ |
| $J$ | 3－M | XA 7－19 | TB 2－38 | XA 1－10 | XA $2-\mathrm{R}$ | J 4－F | XA 4－E | J 1 －R |
| J | 3－P | XA 7－1 | TE 2－48 | XA 1－08 | XA 2－S | J 4－H | XA 4－F | XA 4－A |
| $J$ | 3－5 | XA 7－10 | TB 2－4B | $\times 4$ 1－09 | XA $2-1$ | $\times 1$ 6－23 | XA 4－F | TBiB－U1 |
| J | 3－U | XA 7－37 | Tid 2－58 | $\times 4$ 3－4 | XA 2－U | XA 6－18 | XA 4－01 | T618－01 |

Figure 8－25．（1）．Logic Assembly A1（with TIG），interconnection chart（part 1 of 3）．

LOGIC ASSEMBLY AI ( WITH T.I.G.) WIRE LIST


TM 7440-214-15-WL-2- (2)
Fiqure 8-25(2). Logic Assembly A1 (with TIG), interconnection chart (part21 of 3).

LOGIC ASSEMBLY Al (WITH T.I.G.) WIRE LIST

| FROM | TO | FROM | TO | FROM | TO | FROM | TO |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CON -PIN | CON -PIN | CON -P IN | CON - PIN | CON-PIN | CON-PIN | CON -PIIN | CON -PIN |
| xall-10 | XA10-13 | XA13-E | XA10-06 | XA15- W | XA14-15 | Added wimes |  |
| XA11-10 | XA13-F | XA13-F | XA11-10 | XA15- $X$ | XA 6-14 |  |  |
| XA11-11 |  | XA13-H | $\times \mathrm{XA}$ 1-13 | XA15-Y | XA14-09 |  |  |
| XA1I-12 | XA 9-12 | XA13-M | xal0- ${ }^{\text {W }}$ | XA15-Y | XA16-04 |  |  |
| xA11-13 | XA 8-T | XA13-N | XA10-14 | XA15-01 | TBiH-01 |  |  |
| XA11-14 | XA12-21 | XA13-P | XA12- H | XA15-01 | XA16-01 |  |  |
| XA11-15 | XA12-16 | XA13- 1 | XA12-23 | X415-02 | TBiH-02 |  |  |
| XA11-16 | XA12- | XA13- ${ }^{\text {X }}$ | XA12-14 | x415-02 | KA16-02 |  |  |
| XA11-17 | XA12-E | XA13-AA | XA12-02 | XA15-03 | XA 4-20 |  |  |
| XA11-1.8 | XA12-10 | XA13-01 | TB16-01 | xa15-03 | XA16-P |  |  |
| XA11-19 | XA12-08 | XA13-01 | XA14-01 | XA15-04 | XA 3-H |  |  |
| xAll-20 | x A12-05 | XA13-02 | TH16-02 | XA15-05 | XA16-16 |  |  |
| xA11-21 | XA12-19 | XA13-02 | XA14-02 | XA15-07 | J 3-2 |  |  |
| X $411-22$ | XA B-20 | XA13-03 | XA11-P | XA15-08 | J 3-Y |  |  |
| XA11-23 | XA 9-23 | XA13-04 | XA 9- 2 | X415-09 | XA 1-14 |  |  |
| XAL2-A | XA12-D | XA13-05 | XA11- 2 | XA15-10 | S 1-NO |  |  |
| XA12-A | xA12-07 | XA13-06 | XA10-12 | xa15-11 | XA 3-20 |  |  |
| XA12-B | $\times \mathrm{AlI}=\mathrm{B}$ | XA13-07 | XA 7-15 | XA15-12 | XA 4-22 |  |  |
| XA12-C | XA11- ${ }^{\text {( }}$ | XA13-08 | XA 7-V | XA15-12 | XA16-23 |  |  |
| XA12-0 | XA12-A | XA13-04 | XA12-03 | XA15-13 | J 3-W |  |  |
| XA12-D | xA12- U | XA13-10 | $X A 7-x$ | XA15-14 | XA16-2 |  |  |
| XA12-E | $\times$ (11-17 | XA13-13 | XA 7-12 | XA15-15 | XA14- X |  |  |
| xal2-F | $\times$ X ${ }^{\text {x }}$ (1-08 | XA13-14 | XA10-15 | XA15-16 | xa 2-f |  |  |
| XA12-H | $\times \mathrm{AlO}-\mathrm{H}$ | XA13-15 | XA12- N | XA15-16 | xA16-t |  |  |
| XA12-H | XAI3-P | X413-16 | XA12- J | XA15-17 | XA 4-12 |  |  |
| XA12-J | XA10-J | XA13-17 | $x$ ¢ 7 -22 | XA15-18 | X414-06 |  |  |
| xal2-J | XA13-16 | XA13-18 | XA12-20 | XA15-19 | XA 6-09 |  |  |
| XA12-K | XA11- S | XA13-19 | XA 7- M | XA15-20 | XA 4-08 |  |  |
| kalz-L | x411-05 | XA13-20 | XA12- m | XA15-21 | XA14-W |  |  |
| KA12-M | x411-04 | XA13-21 | XA12-15 | X $\mathrm{A}_{1}$ 5-21 | XA16-N |  |  |
| XA12-N | $\times \mathrm{AlO-N}$ | XA13-22 | XA12- 1 | XA15-22 | XA 6-20 |  |  |
| XA12-N | xA13-15 | XA13-23 | XA10-03 | XA15-23 | XA14-19 |  |  |
| XA12-P | XALI-R | XA14-A | XA13-4 | XA15-23 | XA16-19 |  |  |
| XA12-R | XAIL- C | XA14- ${ }^{\text {¢ }}$ | XA13- B | XA16-A | XA15-A |  |  |
| XA12-S | xAll-K | XA14-0 | $\times \mathrm{A}$ 1- U | XA16-B | XA15-B |  |  |
| XA12-T | XA10- 1 | XA14-H | XA $7-J$ | XAlb-C | XA14-08 |  |  |
| xAl2- | XA13-22 | XAl4- R | XA15-K | XA16-0 | XA15-R |  |  |
| XA12-U | XA12- ${ }^{\text {P }}$ | XA14-S | XA 8-K | XA16-E | XA15-16 |  |  |
| xA12-V | XAll- H | XA14-V | XA 3-F | XAIG- F | XA 4-0 |  |  |
| XAL2-W | XA13-20 | XA14-W | KA 7-06 | XA16- H | XA15- ${ }^{\text {d }}$ |  |  |
| xal2- x | TB1F-01 | XA14- W | XA15-21 | XA16-K | J 2-H |  |  |
| xA12- $x$ | XA12-13 | XA14- X | XA15-15 | XA16- ${ }^{\text {N }}$ | XA15-21 |  |  |
| KAl2- Y | XAll-N | XA14- 2 | XA16-20 | XA16-P | X415-03 |  |  |
| KA12- $Z$ | xA11-16 | XA14-01 | XA13-01 | XA16- R | J 2-R |  |  |
| XA12-AA | XAll-M | XA14-02 | XA13-02 | XA16- ${ }^{\text {P }}$ | J 2-N |  |  |
| xA12-01 | XA12-06 | XA14-05 | XA 7-03 | XA16- ${ }^{\text {( }}$ | J 2-W |  |  |
| <412-02 | XA1J-02 | XA14-06 | XA 2-05 | XA16- X | XA15-L |  |  |
| xa12-02 | XA13-AA | X $\times 14$-06 | XA15-18 | XA16- Y | XA 3-K |  |  |
| xA12-03 | XA13-09 | XA14-08 | XA 3- 0 | XA16-2 | XA15-14 |  |  |
| $\times \mathrm{A} 12-04$ | $\times$ ¢ 8-11 | XA14-08 | XA16-C | XA16-AA | J 2-J |  |  |
| xa12-05 | XA11-20 | XA14-09 | XA15- Y | XA16-01 | XA15-01 |  |  |
| xA12-06 | X A12-01 | XA14-10 | XA 2-09 | $\times 416-02$ | XA15-02 |  |  |
| xA12-06 | xA12-13 | X $\times 14$-10 | XA15- | XA16-03 | XA15-N |  |  |
| xA12-07 | XAlI- ${ }^{\text {P }}$ | XA14-14 | XA15-1 | $\times 416$-04 | XA15-Y |  |  |
| XA17-07 | XA12-A | XA14-15 | KA15- m | XA16-05 | XA 3-16 |  |  |
| xA12-i)8 | KA11-19 | XA14-19 | XA 1- 1 | XA16-06 | XA 3-E |  |  |
| XA12-09 | $\times$ - 11-02 | XA14-19 | XA15-23 | XA16-07 | XA14-20 |  |  |
| XA12-10 | XA11-18 | XA14-20 | XA16-07 | XA16-08 | XA 4-16 |  |  |
| xal2-11 | XA11-03 | XA14-23 | XA 3-19 | XA16-10 | XALS-F |  |  |
| XA12-12 | $\mathrm{x} 411-06$ | XA15-A | T81H-01 | XA16-11 | J 2-L |  |  |
| XA12-13 | XA12-06 | XA15-A | XA16-4 | XA16-12 | J $2-K$ |  |  |
| XA12-13 | XA12- X | XA15- 8 | TBLH-02 | XA16-13 | J 2-F |  |  |
| x412-14 | XA13- X | XA15- ${ }^{\text {P }}$ | XA16-8 | XA16-14 | XA 3-15 |  |  |
| xA12-15 | XA13-21 | XA15-C | XA 4-10 | XA16-15 | XAL5-H |  |  |
| XA12-16 | XA11-15 | XA15- D | XA 2-06 | XA16-16 | XA15-05 |  |  |
| XA12-17 | XA11-V | XA15- D | XA16-H | XA16-17 | J 2-p |  |  |
| XA12-18 | XAll-J | XA15-E | XA 3-17 | XA16-18 | $J$ 2-M |  |  |
| XA12-19 | xall-21 | XA15-F | XA 4-18 | XA16-19 | XA15-23 |  |  |
| XA12-20 | $\times \mathrm{AlO}$ - 0 | XA15-F | XA16-10 | XA16-20 | XA14-2 |  |  |
| XA12-20 | XA13-18 | XA15- H | XA 3-14 | XA16-21 | XA 4-23 |  |  |
| X ${ }^{\text {1 12-21 }}$ | $\times$ (11-14 | XA15-H | XA16-15 | XA16-22 | J 2-x |  |  |
| xA12-22 | XA11-L | XA15-K | X 144 R | XA16-23 | XA15-12 |  |  |
| x412-23 | KA10-23 | XA15-L | XA14-14 |  |  |  |  |
| XA12-23 | XA13- ${ }^{\text {- }}$ | XA15- L | XA16- X |  |  |  |  |
| XA13-A | TBIG-01 | XA15-M | XA 3-J |  |  |  |  |
| XA13-A | XA14-A | XA15-N | XA 3-21 |  |  |  |  |
| XA13- B | TBIG-02 | XA15- N | XA16-03 |  |  |  |  |
| XA13- B | XA14-B | XA15-R | XA16-0 |  |  |  |  |
| $\times \mathrm{AL3}-\mathrm{C}$ | XA 7-21 | XA15- 1 | XA14-10 |  |  |  |  |
| XA13-0 | $\times 410-08$ | XA15-U | XA 3-18 |  |  |  |  |

## REFERENCES

The following publications apply to operation and maintenance of the equipment covered in this manual:

DA Pam 310-4
DA Pam 310-7
NW 00-15PA-1
SB38-100
TB SIG 222
TB 43-0118

TM 38-750
TM 11-7440-238-15/
NAVELEX 0967-LP-
324-0100/TO 31W4-
4-1-101
TM 11-7440-239-15/
NAVELEX 0967-LP-
324-0110/TO 31W4-
4-1-111
T.O. 00-25-234

TM 750-244-2
TB SIG 355-1
TB SIG 355-2
TB SIG 355-3
TM 740-0-1
TM 750-244-2

Index of Technical Manuals, Technical Bulletins, Supply Manuals (types 7, 8, and 9), Supply Bulletins, and Lubrication Orders.
U.S. Army Equipment Index of Modification Work Orders. Technical Inspection Manual, Soldering for Electric and Electronic Application (Navy)
Preservation, Packaging, Packing and Marking Materials, Supplies, and Equipment Used by the Army.
Solder and Soldering
Field Instructions for Painting and Preserving Electronics Command Equipment, Including Camouflage Pattern Painting of Electrical Equipment Shelters.
The Army Maintenance Management System (TAMMS)
Operator's Organizational, Direct Support, General Support, and Depot Maintenance Manual, Digital Subscriber Terminals AN/FYA-71(V)1 Through AN/FYA-71(V) 6 and Device Switch Module SA-1616/G

Operator's Organizational, Direct Support and Depot Maintenance Manual, Autodin Digital Subscriber Terminals (Station Manual)

General Shop Practice Requirements for the Repair, Maintenance, and Test of Electronic Equipment.
Procedures for Destruction of Electronics Material to Prevent Enemy Use (Electronics Command).
Depot Inspection Standard for Repaired Signal Equipment.
Depot Inspection Standard for Refinishing Repaired Signal Equipment.
Depot Inspection Standard for Moisture and Fungus Resistant Treatment.
Administrative Storage of Equipment
Procedure for Destruction of Electronics Materiel to Prevent Enemy Use.

## Change 7 A-1

## APPENDIX C

 MAINTENANCE ALLOCATION
## Section I. INTRODUCTION

## C-1. General

This appendix provides a summary of the maintenance operations covered in the equipment maintenance manual for Reader, Punched Tape RP-154(P)/'G. It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function.
This appendix may be used as an aid in planning maintenance operations.

## C-2. Explanation of Format for Maintenance Allocation Chart

a. Group Number. Group numbers correspond to the reference designation prefix assigned in accordance with ASA Y32.16, Electrical and Electronics Reference Designations. They indicate the relation of listed items to the next higher assembly.
b. Component Assembly Nomenclature. This column lists the item names of component units, assemblies, subassemblies, and modules on which maintenance is authorized.
c. Maintenance Function. This column indicates the maintenance category at which performance of the specific maintenance function is authorized. Authorization to perform a function at any category also includes authorization to perform that function at higher categories. The codes used represent the various maintenance categories as follows:

Code Maintenance category
C........................................Operator/crew
H......................................General support maintenance
D.......................................Depot maintenance
d. Tools and Equipment. The numbers appearing in this column refer to specific tools and equipment which are identified by these numbers in section III.
e. Remarks. Self-explanatory.

## C-3. Explanation of Format for Tool and Test Equipment Requirements

The columns in the tool and test equipment requirements chart are as follows:
a. Tools and Equipment. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool for the maintenance function.
b. Maintenance Category. The codes in this column indicate the maintenance category normally allocated the facility.
c. Nomenclature. This column lists tools, test, and maintenance equipment required to perform the maintenance functions.
d. Federal Stock Number. This column lists the Federal stock number.
e. Tool Number. Not used.


TM 11-7440-219-15/NAVSHIPS 0967-324-0052/TO 31W4-2G-61
SECTION III. TOOL AND TEST EQUIPMENT REQUIREMENTS
TOOLS AND TEST EQUIPMENT REQUIREMENTS


## APPENDIX D

ON-SITE. AREA RESUPPLY, AND DEPOT REPAIR PARTS

## Section I. INTRODUCTION

## D-1. Scope

a. The equipment covered in this appendix is categorized as a "FIXED STATION INSTALLATION." Maintenance functions have been authorized to site (ORG thru GSU), Area Resupply, and depot.
$b$. This equipment is used by electronic service organizations organic to the theater headquarters or communications zones to provide theater communications. Those repair parts authorized up to and including general support maintenance are to be stocked by the organization operating this equipment, therefore a separate display of "Organizational" and "Direct Support" maintenance repair parts would be repetitious and are not included in this appendix.

## D-2. General

a. The Prescribed Load Allowance (PLA) is not required since this information is adequately defined under "Site Stockage Allowance," Column 7.
b. This list includes all replaceable parts and defines repair parts authorized for maintenance performance at site (ORG and GSU) and depot categories. This list also includes allowances for prepositioned resupply of repair parts based on equipment density per geographical locations.
This resupply requirement is established to sum port each Military Department's concentration of DSTE devices to meet the Defense Communication System operational requirement.
c. The repair parts listing is preceded with a crossreference index.

## D-3. Explanation of Columns

An explanation of the columns is given below:
a. Source, Maintenance, and Recoverability Codes (SMR), Column 1. This column lists the applicable SMR codes for the part as follows:
(1) Source code (A). The source code indicator is the letter appearing on the left in the SMR column. It indicates the source from which the item is obtained in accordance with the following:

## NOTE

See para D-3 (4) for cross-reference to Air Force SMR codes.

Code
Explanation
P- Applies to repair parts that are stocked in or supplied from the GSA/DSA, or Army supply system, and authorized for use at indicated maintenance categories
M- Applies to repair parts that are not procured or stocked but are to be manufactured at indicated maintenance categories.
A- Applies to assemblies that are not procured or stocked as such but are made up of two or more units, each of which carries an individual stock number and description and is procured and stocked and can be assembled by units at indicated maintenance categories.
X- Applies to parts and assemblies that are not procured or stocked; the mortality of which normally is below that of the applicable end item; and the failure of which should result in retirement of the end item from the supply system
X1- Applies to repair parts that are not procured or stocked, the requirement for which will be supplied by the use of next higher assembly or component
X2- Applies to repair parts that are not stocked. The indicated maintenance category requiring such repair parts will attempt to obtain them through cannibalization; if not obtainable through cannibalization; such repair parts will be requisitioned with supporting Justification through normal supply channels.
C Applies to repair parts authorized for local procurement If not obtainable from local procurement, such repair parts will be requisitioned through normal supply channels with a supporting statement of nonavailability from local procurement.
G- Applies to major assemblies that are procured with PEMA funds for initial issue only to be used as exchange assemblies at DSU and GSU category. These assemblies will not be stocked
above DSU and GSU category or returned to depot supply category.
(2) Maintenance code (B). The maintenance code indicator is the letter appearing in the center of the SMR column. It indicates the lowest category of maintenance authorized to install the listed item. The codes are:
Code

## Explanation

*C.............................Operator/Crew
*O.............................Organizational Maintenance
*F .............................Direst Support Maintenance
H ................................General Support Maintenance
D ...............................Depot Support Maintenance
NOTE
Codes "C" "0" and "F" have not been utilized in this manual. Site maintenance functions have been designated " H " which includes "C" through "F".
(3) Recoverability code (C). The third, or right hand letter in the SMR column indicates whether the item should be returned for recovery or salvage.
Recoverability codes and their explanations are as follows:

## NOTE

When no code is indicated in the recoverability column, the part will be considered expendable
Code
Explanation
R- Applies to repair parts and assemblies which are economically repairable at DSU and GSU activities and normally are furnished by supply on an exchange basis.
T- Applies to high dollar value recoverable repair parts which are subject to special handling and are issued on an exchange basis. Such repair parts normally are repaired or overhauled at depot maintenance activities.
U- Applies to repair parts specifically selected for salvage by reclamation units because of precious metal content, critical materials, high dollar value reusable casing or castings.
(4) Cross-reference Army to Air Force SMR code. The following SMR codes represent a cross reference from Army SMR codes displayed in this appendix to appropriate Air Force SMR codes. This coding has been coordinated with OCAMA symbol OCNDTB.

| ARMY SNMR |  |  |  |  | REPAIR NEVMEL <br> (AFLCR |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PH | $\mathbf{P}$ | 1 | - | N | $\mathbf{s}$ | - |
| PHR | $\mathbf{P}$ | 1 | - | T | D | - |
| PHT | $\mathbf{P}$ | 1 | - | T | D |  |
| PD | P | 1 | D | N | 8 | - |
| PDR | $\mathbf{P}$ | 1 | - | T | D | - |
| X1H | X | 1 | - | - | F | - |
| X1D | I | 1 | E | - | D | - |
| ${ }_{\text {AR }}$ | A | 2 | - | - | ${ }_{5}$ | - |
| AFR | A | - | - | - | $F$ | - |
| C | L | - | F | - | - | - |
| G | G | - | - | - | - | - |
| ME | M | - | - | - | E | - |
| MD | $\mathbf{M}$ | - | - | - | D | - |

b. Federal Stock Number, Column 2. The Federal stock number for the item is listed in this column. (see "Note" at end of Appendix D
c. Description, Column 3. This column includes a sequence number, the federal item name, a five-digit Federal supply code for Manufacturer's an indenture code and a part number. The five-digit Federal supply code is followed by the manufacturer's part number. For subsequent appearances of the same item, the manufacturer's code and part number are omitted. The words "same as" followed by the index number assigned to the item when it first appeared in the list will follow the item name, e.g., "RESISTOR, FIXED, COMPOSITION: SAME AS A298." Model column is not used.
d. Unit of Issue, Column 4. The unit used as a basis of issue (e.g., ea, pr, ft, yd, etc.) is indicated in this column.
e. Quantity Incorporated in Unit Pack, Column 5. Not used.
f. Quantity Incorporated in Unit, Column 6. The total quantity of the item used in the equipment is given in this column. Subsequent appearances of the same item in the same any are indicated by the letters "REF".
g. Site Stockage Allowance, Column 7.
(1) The maintenance allowance column are divided into subcolumns. The total quantity of items authorized for the number of equipments supported is indicated in each subcolumn oppo

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site the first appearance of each item. Subsequent appearances of the same item will have no entry in the allowance columns but will have a reference in the description column to the first appearance of the item. Items authorized for use as required, but not for initial stockage, are identified with an asterisk (*) in the allowance column.
(2) The quantitative allowances for Site (ORG thru GSU) maintenance represents one initial prescribed load for the number of equipments supported.
(3) Subsequent changes to Site (ORG thru GSU), allowances will be limited as follows: No change in the range of items is authorized. If additional items are considered necessary, recommendation should be forwarded to Commanding General, U. S. Army Electronics Command, ATTN: AMSELME-NMP-CW, Fort Monmouth, N. J. 07703, for exception or revision to the allowance list. Revisions to the range of items authorized will be made by USAECOM National Maintenance Point based upon engineering experience, demand data, or TAERS information.
h. Forty-five Day Area Resupply Allowance Based on Number of DSTE Devices Supported, Column 8.
(1) The allowance column is divided into three subcollumns. The total quantity of items authorized for the number of equipments supported is indicated in each subcolumn opposite the first appearance $6 f$ each item.
(2) The quantitative resupply allowances for the area resupply, represents one initial prescribed load for the number of DSTE equipments to be supported.
(3) Subsequent changes to Area Resupply

## NOTE:

1. Effective 30 September 1974, all Federal Stock Numbers listed in the following On-Site, Area Resupply, and Depot Parts List were converted to the 13-digit National Stock Number (NSN) System.
2. To obtain the 13 -digit NSN by conversion from the 11-digit Federal Stock Number, a National Codification Bureau Code (NCBC) of "00" will be entered following the Federal Stock Classification (FSC) code (first four digits).
allowances will be limited as follows: No change in the range of items is authorized. If additional items are considered necessary, recommendation should be forwarded to Commanding General, U. S. Army Electronics Command, ATTN: AMSEL-ME-NMP-CW, Fort Monmouth, N. J. 07703, for exception or revision to the allowance list. Revisions to the range of items authorized will be made by USAECOM National Maintenance Point based upon engineering experience, demand data, or TAERS information.
i. One-Year Allow? 4 ances Per 100

Equipments/ Contingency Planning Purposes, Column 9. Contingency planning requirements must be computed on a per equipment basis for fixed plant equipment, therefore column 9 will not be utilized. Contingency Plan requirements for this equipment will be satisfied by furnishing 1 load of repair parts per quantities displayed under column 7 Site Stockage Allowance.
j. Depot Maintenance Allowance per 100 Equipments, Column 10. This column indicates the total quantity of each item authorized depot maintenance for 100 equipments. Subsequent appearances of the same item will have no entry in this column, but will have a reference in the description column to the first appearance of the item.
k. Illustrations, Column 11.
(1) Figure number, column 11a. The number of the illustration in which the item is shown is indicated in this column.
(2) Item No. or reference designation, column 11b. The callout number or reference designation used to reference the item in the illustration appears in this column.
3. An example of coding and expansion of the FSN to the NSN is as follows:
a. FSN - 6625-553-0142
b. ,CBC - 00
c. FSC-6625
d. SEN - 6625-00-553-0142
4. All replacement parts will be ordered under the ISN System.

## SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER



## SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER

| FIG. NO. | ITEM NO. OR <br> REFERENCE DESIGNATION | INDEX NO. | FIG. NO. | ITEM NO. OR REFERENCE DESIGNATION | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4-5 | 90 | B854 |  | 10 | A085B |
|  | 91 | B855 |  | 11 | A090B |
|  | 92 | B856M |  | 12 | A095B |
|  | 93 | 8857 |  | 13 | A100B |
|  | 94 | B858 |  | 14 | A105B |
|  | 95 | B859 |  | 15 | A110B |
|  | 96 | B862A |  | 16 | A115B |
|  | 97 | B862B |  | 17 | A120M |
|  | 98 | 8860 |  | 18 | A121 |
|  | 99 | B862D |  | 19 | A121B |
|  | 100 | B879 |  | 20 | A121C |
|  | 101 | B893A |  | 21 | A121D |
|  | 102 | B906A |  | 22 | A121A |
|  | 103 | B894B |  | 23 | A130A |
|  | 104 | B938 |  | 24 | A130B |
|  | 105 | B941 |  | 25 | A130C |
|  | 106 | B958 |  |  |  |
|  | 107 | B957A | 4-7 | 1 | B457A |
|  | 108 | B960 |  | 2 | B459 |
|  | 109 | B959 |  | 3 | B458A |
|  | 110 | 8978 |  | 4 | B456 |
|  | 111 | B979 |  | 5 | B455 |
|  | 112 | B980 |  | 6 | B461A |
|  | 113 | B981 |  | 7 | B4GIB |
|  | 114 | B977 |  | 8 | B461C |
|  | 115 | B983 |  | 9 | P453 |
|  | 116 | 8995 |  | 10 | B454 |
|  | 117 | B985 |  | 11 | B461 |
|  | 118 | B984 |  |  |  |
|  | 119 | B982 | 4-8 | 1 | B102 |
|  | 120 | B986 |  | 2 | B397 |
|  | 121 | B990 |  | 3 | B142 |
|  | 122 | C013 |  | 3.1 | B208A |
|  | 123 | C017 |  | 4 | A938 |
|  | 124 | C029 |  | 4.1 | B101A |
|  | 125 | C039 |  | 5 | B209 |
|  | 126 | C042 |  | 6 | B235 |
|  | 127 | C050 |  | 7 | A830 |
|  | 128 | C51 |  | 8 | A902 |
|  | 129 | C052 |  | 9 | A872 |
|  | 130 | C049 |  | 10 | A849 |
|  | 131 | C057 |  | 11 | B334 |
|  | 132 | C058 |  | 12 | B366 |
|  | 133 | C059 |  | 13 | B287 |
|  |  |  |  | 14 | 8406 |
| 4-6 | 1 | A033 |  | 15 | B446 |
|  | 2 | A039 |  | 15.1 | B446A |
|  | 3 | A045 |  | 16 | B443 |
|  | 4 | A051 |  | 17 | B444 |
|  | 5 | A056 |  | 18 | B445 |
|  | 6 | A061 |  | 19 | B409 |
|  | 7 | A067 |  | 20 | B410 |
|  | 8 | A073 |  | 21 | B411 |
|  | 9 | A079 |  | 22 | B408 |

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## SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER

| FIG. NO. | ITEM NO. OR REFERENCE DESIGNATION | $\begin{gathered} \text { INDEX } \\ \text { NO. } \end{gathered}$ | FIG. NO. | ITEM NO. OR <br> REFERENCE DESIGNATION | INDEX NO. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4-8 | 23 | B447A | 4-9 | 1 | B815 |
|  | 23.1 | B442 |  | 2 | B818 |
|  | 24 | B430 |  | 3 | B816 |
|  | 25 | B431 |  | 4 | B817M |
|  | 26 | 8432 |  | 5 | B820 |
|  | 27 | B431A |  | 6 | B814A |
|  | 28 | B428B |  | 7 | B819 |
|  | 29 | B429 |  | 8 | B803 |
|  | 30 | B435 |  | 9 | B80SA |
|  | 31 | B436 |  | 10 | B804 |
|  | 32 | B437 |  | 11 | B807 |
|  | 33 | B436A |  | 12 | B813 |
|  | 34 | B433A |  | 13 | B802A |
|  | 35 | B434 |  | 14 | B806 |
|  | 36 | B415 |  | 14.1 | B821B |
|  | 37 | B417 |  | 14.2 | B821D |
|  | 38 | B418 |  | 14.3 | B821C |
|  | 39 | B416 |  | 14.4 | B821A |
|  | 40 | B426 |  | 14.5 | B823 |
|  | 40.1 | B414 |  | 14.6 | B824 |
|  | 40.2 | B426C |  | 14.7 | B832 |
|  | 40.3 | B426B |  | 15 | B821 |
|  | 40.4 | B426D |  |  |  |
|  | 40.5 | B426E | 4-10 | 1 | A720B |
|  | 40.6 | B426F |  | 2 | A720D |
|  | 40.7 | B426G |  | 3 | A720C |
|  | 40.8 | B426H |  | 4 | A720A |
|  | 40.9 | B426I |  | 4.1 | A721A |
|  | 41 | B420 |  | 5 | A753 |
|  | 42 | B421 |  | 5.1 | A753A |
|  | 43 | B419 |  | 6 | A740 |
|  | 43.1 | B425A |  | 7 | A745 |
|  | 44 | B423 |  | 8 | A741 |
|  | 45 | B425 |  | 9 | A746A |
|  | 46 | B424 |  | 10 | A749A |
|  | 47 | B422 |  | 11 | A733B |
|  | 48 | B426K |  | 12 | A736B |
|  | 49 | B411B |  | 13 | A727A |
|  | 50 | B411C |  | 14 | A729A |
|  | 51 | B411D |  | 15 | A781 |
|  | 52 | B411E |  | 16 | A783 |
|  | 52.1 | B411K |  | 17 | A782 |
|  | 52.2 | B440A |  | 18 | A780 |
|  | 52.3 | B411F |  | 19 | A723A |
|  | 52.4 | B411G |  | 20 | A722A |
|  | 52.5 | B411J |  | 21 | A776 |
|  | 52.6 | B411H |  | 22 | A778 |
|  | 53 | B411A |  | 23 | A777 |
|  | 54 | B441 |  | 24 | A775A |
|  | 55 | B427 |  | 25 | A793A |
|  | 56 | B407 |  | 26 | A792A |
|  | 57 | B412A |  | 27 | A796A |
|  | 58 | B413A |  | 28 | A801 |
|  | Change 4 D-6 |  |  |  |  |

## SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER

| FIG. NO. | ITEM NO. OR REFERENCE DESIGNATION | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ | FIG. <br> NO. | ITEM NO. OR REFERENCE DESIGNATION | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4-10 | 29 | A803 |  | 74 | A822 |
|  | 30 | A802 |  | 75 | A820B |
|  | 31 | A806A |  | 76 | A8201 |
|  | 32 | A800A |  | 77 | A813 |
|  | 33 | ABOSM |  | 78 | A815E |
|  | 34 | A772 |  | 78.1 | A815C |
|  | 35 | A774 |  | 78.2 | A815B |
|  | 36 | A773 |  | 78.3 | A815A |
|  | 37 | A771 |  | 78.5 | A819A |
|  | 38 | A770 |  | 79 | A815 |
|  | 39 | A769 |  | 80 | A814 |
|  | 40 | A489A |  | 81 | A812 |
|  | 41 | A142A |  | 82 | A816A |
|  | 42 | A114A |  | 83 | A695A |
|  | 43 | A144 |  | 83.1 | A696 |
|  | 44 | A1143M |  | 83.2 | A698 |
|  | 45 | A141A |  | 83.3 | A697 |
|  | 45.1 | A15SA |  | 84 | A694A |
|  | 46 | A145 |  | 84.1 | A672B |
|  | 47 | A1S1 |  | 85 | A673 |
|  | 48 | A140 |  | 86 | A67S |
|  | 49 | A139 |  | 87 | A674 |
|  | s | A163A |  | 88 | A672.A |
|  | 51 | A164B |  | 89 | A756 |
|  | 52 | A164C |  | 90 | A7S8 |
|  | 53 | A162A |  | 91 | A757 |
|  | 54 | A164A |  | 92 | A172B |
|  | 55 | A157M |  | 93 | A210B |
|  | 56 | A158 |  | 94 | A279B |
|  | 57 | A160 |  | 95 | A754 |
|  | 58 | A161A |  | 96 | A7SS |
|  | 59 | A318 |  | 97 | A828A |
|  | 60 | A320 |  | 98 | A828C |
|  | 61 | A319 |  | 99 | A828B |
|  | 62 | A317A |  | 100 | A826 |
|  | 62.1 | A321A |  | 101 | A828 |
|  | 62.2 | A322 |  | 102 | A827M |
|  | 62.3 | A324 |  | 103 | A825A |
|  | 62.4 | A323 |  | 104 | A166A |
|  | 62.5 | A329A |  | 105 | A167 |
|  | 62.6 | A330A |  | 106 | A168 |
|  | 62.7 | A331 |  | 107 | A169A |
|  | 62.8 | A333 |  | 108 | A170 |
|  | 62.9 | A332 |  | 109 | A171 |
|  | 62.10 | A385A |  | 110 | A165B |
|  | 62.11 | A461A |  | 111 | A172 |
|  | 63 | A789 | 4-11 |  |  |
|  | 64 | A791 |  | 1 | A026 |
|  | 65 | A790 |  | 2 | A027A |
|  | 66 | A788 |  | 3 | A028A |
|  | 67 | A785 |  | 5 | A006 |
|  | 68 | A787 |  | 6 | A019 |
|  | 69 | A786 |  | 7 | A018 |
|  | 70 | A78A4 |  | 8 | A021 |
|  | 9 | AO20M |  |  |  |
|  | 72 | A821 |  |  |  |
|  | 73 | A823 |  |  |  |

[^3]SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE
TO INDEX NUMBER TO INDEX NUMBER

| FIG. NO. | ITEM NO. OR <br> REFERENCE DESIGNATION | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ | $\begin{aligned} & \text { FIG. } \\ & \text { NO. } \end{aligned}$ | ITEM NO. OR REFERENCE DESIGNATION | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4-11 | 11 | A017 |  | 22 | B743 |
|  | 12 | A013 |  | 23 | B742 |
|  | 13 | A012 |  | 23.1 | B741 |
|  | 14 | A015 |  | 24 | B727B |
|  | 15 | A014B |  | 25 | B727 |
|  | 16 | A010A |  | 26 | B726 |
|  | 17 | A011 |  | 27 | 87258 |
|  | 18 | A005A |  | 28 | B725 |
|  |  |  |  | 29 | B722B |
| 4-11.1 | 1 | B966 |  | 30 | B721B |
|  | 2 | B968 |  | 31 | B721A |
|  | 3 | B971 |  | 32 | B720 |
|  | 4 | B972 |  | 33 | B723D |
|  | 5 | B970 |  | 34 | B723E |
|  | 6 | B973 |  | 35 | B724A |
|  | 7 | B974 |  | 36 | B715E |
|  | 8 | B975 |  | 37 | B715F |
|  | 9 | B976 |  | 38 | B715C |
|  | 10 | B965 |  | 39 | B719 |
|  |  |  |  | 40 | B716 |
| 4-11.2 | 1 | B839D |  | 40.1 | B715A |
|  | 2 | B839E |  | 41 | B715 |
|  | 3 | B839F |  | 42 | B723 |
|  | 4 | B839G |  | 43 | B713A |
|  | 5 | B839C |  | 43.1 | B713B |
|  | 6 | B839B |  | 44 | B714A |
|  |  |  |  | 45 | B712 |
| 4-12 | 1 | B740A |  | 46 | B659A |
|  | 2 | B739 |  | 47 | B658 |
|  | 3 | B737A |  | 48 | B657 |
|  | 4 | B738 |  | 49 | B656A |
|  | 4.1 | B738C |  | 50 | B656 |
|  | 4.2 | B738B |  | 51 | 8655 |
|  | 4.3 | B738D |  | 52 | 8619A |
|  | 4.4 | B738A |  | 53 | B620 |
|  | 5 | B736 |  | 54 | B618 |
|  | 6 | B735 |  | 55 | B617 |
|  | 7 | B734 |  | 56 | B616 |
|  | 8 | B7338 |  | 58 | B613A |
|  | 8.1 | B733D |  | 59 | BS549 |
|  | 9 | B733C |  | 60 | B483 |
|  | 10 | B732A |  | 61 | B482M |
|  | 11 | B730A |  | 62 | B551A |
|  | 12 | 8731A |  | 63 | 8552 |
|  | 12.1 | B731B |  | 63.1 | B552A |
|  | 13 | B729 |  | 64 | B550 |
|  | 14 | B728 |  | 65 | B548A |
|  | 15 | B749 |  | 66 | B547A |
|  | 16 | B748A |  | 67 | B546A |
|  | 17 | B747 |  | 68 | B546 |
|  | 18 | 8746 |  | 68.1 | B7508 |
|  | 19 | 8745A |  | 69 | BS535 |
|  | 20 | B745M |  | 70 | BS534 |
|  | 21 | B744A |  | 71 | B533A |

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## SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER

| FIG. <br> NO. | ITEM NO. OR REFERENCE DESIGNATION | $\begin{gathered} \text { INDEX } \\ \text { NO. } \end{gathered}$ | $\begin{aligned} & \text { FIG. } \\ & \text { NO. } \end{aligned}$ | ITEM NO. OR REFERENCE DESIGNATION | $\begin{aligned} & \text { INDEX } \\ & \text { NO. } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4-12 | 72 | B537A |  | 6 | 8703 |
|  | 73 | B5539 |  | 7 | B704 |
|  | 74 | B538M |  | 8 | B704B |
|  | 75 | B8536 |  | 9 | B705 |
|  | 76 | B531A |  | 10 | 8701 |
|  | 77 | B532 |  | 11 | B700 |
|  | 78 | B530 |  | 11.1 | B697A |
|  | 78.1 | B532A |  | 12 | B686A |
|  | 78.2 | B532C |  | 13 | B687 |
|  | 78.3 | B532D |  | 13.1 | B687A |
|  | 78.4 | B532B |  | 13.2 | B6878 |
|  | 78.5 | B532E |  | 13.3 | B687C |
|  | 79 | B504 |  | 13.4 | B687D |
|  | 80 | B506 |  | 14 | B690 |
|  | 81 | B507A |  | 15 | B688 |
|  | 82 | B505A |  | 16 | B695A |
|  | 83 | B479 |  | 19 | B689 |
|  | 84 | B481 |  | 19.1 | B685A |
|  | 86 | B480A |  | 20 | B684 |
|  | 87 | B514M |  | 21 | B683 |
|  | 88 | B513M |  | 22 | B682M |
|  | 89 | B515 |  | 23 | B681 |
|  | 90 | B508 |  | 24 | B680 |
|  | 91 | B511A |  | 24.1 | B680A |
|  | 92 | B512 |  | 24.2 | B680B |
|  | 93 | B529A |  | 25 | B679 |
|  | 93.1 | B503 |  | 26 | B678 |
|  | 94 | B481A |  | 27 | B677 |
|  | 95 | B475A |  | 28 | B676A |
|  | 96 | B477 |  | 29 | B675 |
|  | 98 | B474 |  | 30 | B672.A |
|  | 99 | B473 |  | 31 | B671 |
|  | 100 | B472A |  | 33 | B668 |
|  | 100.1 | B472C |  | 34 | B667 |
|  | 100.2 | B472B |  | 35 | B666 |
|  | 101 | B471A |  | 36 | B665M |
|  | 102 | B469A |  | 37 | B664M |
|  | 103 | B470 |  | 38 | B663 |
|  | 104 | B468 |  | 39 | B662 |
|  | 105 | B467 |  | 39.1 | B661A |
|  | 106 | B502 |  | 39.2 | B662A |
|  | 107 | B466M |  | 39.3 | B662B |
|  | 108 | B465 |  | 40 | B711C |
|  | 109 | B464M |  | 41 | B711B |
|  | 110 | B463 |  | 43 | B709 |
|  | 111 | B462 |  | 44 | B710D |
|  | 112 | B717A |  | 44.1 | B710E |
|  |  |  |  | 45 | B710F |
| 4-13 | 1 | B698A |  | 46 | B710A |
|  | 2 | B699 |  | 47 | B660A |
|  | 2.1 | B699A |  |  |  |
|  | 3 | B707 |  | 49 | B711D |
|  | 4 | B706 |  |  |  |
|  | 5 | B702 | 4-14 | 1 | B635A |
|  |  |  |  | 1.1 | B635B |
|  |  |  |  | 1.2 | B635C |

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## SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER



## SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER



## SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER



## SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER

| FIG. NO. | ITEM NO. OR REFERENCE DESIGNATION | $\begin{gathered} \text { INDEX } \\ \text { NO. } \end{gathered}$ | $\begin{aligned} & \text { FIG. } \\ & \text { NO. } \end{aligned}$ | ITEM NO. OR <br> REFERENCE DESIGNATION | $\begin{gathered} \text { INDEX } \\ \text { NO. } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 5-19 | E8 | A437 |  | H2 | A466 |
|  | E9 | A438 |  | H3 | A467 |
|  | E10 | A439 |  | H4 | A468 |
|  | E11 | A440 |  | H5 | A470A |
|  | E12 | A441 |  | H6 | A479A |
|  | E13 | A442 |  | H7 | A480A |
|  | E14 | A443 |  | H8 | A488 |
|  | E1S | A444 |  | P1 | A469 |
|  | E16 | A445 |  | Q1 | A474 |
|  | E17 | A446 |  | Q2 | A478 |
|  | E18 | A447 |  | R1 | A471 |
|  | E19 | A448 |  | R2 | A472D |
|  | E20 | A449 |  | R3 | A473M |
|  | E21 | A450 |  |  |  |
|  | E22 | A451 | 5-21A | PSIA14 | A672A |
|  | E23 | A452 |  | CR1 | A689 |
|  | E24 | A453A |  | CR2 | A690 |
|  | E25 | A454A |  | CR3 | A691 |
|  | H1 | A389A |  | CR4 | A692 |
|  | H2 | A390 |  | E1 | A677 |
|  | H3 | A391 |  | E2 | A678 |
|  | H4 | A392 |  | E3 | A679 |
|  | HS | A399A |  | E4 | A680 |
|  | H6 | A400M |  | H1 | A681 |
|  | H7 | A415 |  | H2 | A682B |
|  | H8 | A422A |  | H3 | A681A |
|  | H9 | A430C |  | H4 | A684A |
|  | H10 | A430D |  | H5 | A685 |
|  | H11 | A430E |  | H6 | A686 |
|  | H12 | A431A |  | H7 | A686A |
|  | H13 | A432A |  | H8 | A693 |
|  | H14 | A458 |  | H9 | A693A |
|  | P1 | A397 |  | H10 | A693B |
|  | P2 | A398 |  | H11 | A693C |
|  | Q1 | A411 |  | H12 | A694G |
|  | Q2 | A416 |  | JS | A694B |
|  | Q3 | A421 |  | J6 | A694C |
|  | Q4 | A426 |  | J7 | A694D |
|  | RI | A401A |  | J8 | A694E |
|  | R2 | A406M |  | J9 | A694F |
|  | R3 | A403 |  | R1 | A683D |
|  | R4 | A406B |  | R2 | A687A |
|  | RS | A402A |  | R3 | A688A |
|  | R6 | A406A |  |  |  |
|  | R7 | A405M | 5-21B | PSIAI5 | A695A |
|  | C1 | A700 |  |  |  |
| 5-20 |  | A461A |  | C2 | A701 |
|  | E1 | A481 |  | C3 | A702 |
|  | E2 | A482 |  | C4 | A703 |
|  | E3 | A483 |  | C5 | A703A |
|  | E4 | A4B4 |  | CR1 | A716 |
|  | E5 | A485 |  | CR2 | A717 |
|  | E6 | A486 |  | CR3 | A718 |
|  | H1 | A465B |  | CR4 | A719 |
|  | Change 4 D-13 |  |  |  |  |

## SECTION II INDEX-FIGURE AND ITEM NUMBER CROSS REFERENCE TO INDEX NUMBER



## Section III. ON SITE, AREA RESUPPLY, AND DEPOT PARTS LIST

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  | \left.SITE, AREA RESUPPLY,   (4) <br> AINTENANCE   $\right]$ | (6) | (30 DAYS SITE STOCKAGE ALLOWANCE |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW. BASED ON NO. EQUIP. SUPPORTED |  |  | (9) <br> 1 YR. <br> ALW. <br> PER <br> 100 <br> EQUP <br> CNTG <br> CY PL. | $\begin{gathered} \text { (10) } \\ \text { DEPOT } \\ \text { MAINT } \\ \text { ALW. } \\ \text { PER } \\ 100 \\ \text { EQUIP. } \end{gathered}$ | (11) ILLUSTRATIONS |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | $\begin{array}{\|c\|} \hline \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | $\stackrel{(2)}{\text { FEDERAL }}$ stock NUMBER | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, and depot maintenance |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (A) | (B) |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (A) | $\begin{gathered} (\mathrm{B}) \\ 6-10 \end{gathered}$ | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ | $\begin{aligned} & (\mathrm{A}) \\ & 1-5 \end{aligned}$ |  |  |  | $\begin{gathered} \text { (B) } \\ 6-10 \end{gathered}$ |  | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ |  | DESIGN |
|  |  |  | 59627911048 | x | x |  |  |  |  | D | A892 | INTEGRATED CIRCUIT, LOGIC GATE: <br> SAME AS A852 |  | EA |  | REF |  |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-4 \end{gathered}$ | Z6 |
|  |  |  | 59627911048 | X | x |  |  |  |  | D | A893 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A852 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-4$ | Z7 |
|  |  |  | 59627911048 | x | x |  |  |  |  | D | A894 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A852 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-4 \end{aligned}$ | Z10 |
|  |  |  | 59627911048 | x | x |  |  |  |  | D | A895 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A852 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-4 \end{aligned}$ | Z11 |
|  |  |  | 59627911048 | x | x |  |  |  |  | D | A896 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A852 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-4 \end{aligned}$ | Z14 |
|  |  |  | 59627911048 | x | x |  |  |  |  | D | A897 | INTEGRATED CIRCUIT, LOGIC GATE: <br> SAME AS A852 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-4 \end{aligned}$ | Z15 |
|  |  |  | 59627911048 | x | x |  |  |  |  | D | A898 | INTEGRATED CIRCUIT, LOGIC GATE: <br> SAME AS A852 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-4 \end{gathered}$ | Z22 |
|  |  |  | 59627911048 | x | x |  |  |  |  | D | A899 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A852 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-4 \end{aligned}$ | Z23 |
|  |  |  | 59627911048 | X | x |  |  |  |  | D | A900 | INTEGRATED CIRCUIT, LOGIC GATE: <br> SAME AS A852 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-4 \end{aligned}$ | Z26 |
|  |  |  | 59627911048 | x | x |  |  |  |  | D | A901 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A852 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-4 \end{aligned}$ | Z27 |

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| (1) |  |  | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  | $\begin{array}{c\|} \hline \text { (4) } \\ \text { UNIT } \\ \text { OF } \\ \text { ISSUE } \end{array}$ | $\begin{aligned} & \text { (5) } \\ & \text { QTY } \\ & \text { INC } \\ & \text { IN } \\ & \text { UN } \\ & \text { PK } \end{aligned}$ | (6) <br> QTY <br> INC <br> UNIT | (7) 30 DAYS site stockage ALLOWANCE |  |  | 45 DAY(8REARESUPPLY ALLOW.BASED ON NO.EQUIP. SUPPORTED |  |  | (9) <br> 1 YR. <br> ALW. <br> PER <br> 100 <br> EQUIP <br> CNGG <br> CY PL. | (10) <br> DEPOT <br> MANT <br> ALW. <br> PRR <br> 100 <br> EQUIP. | (11) ILLUSTRATIONS |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | (C) <br> REC <br> CODE | $\stackrel{(2)}{\text { FEDERAL }}$ STOCK NUMBER | MODEL |  |  |  |  |  | $\begin{aligned} & \text { IND } \\ & \text { CD } \end{aligned}$ | (3) <br> DESCRIPTION |  |  |  |  |  |  |  | (A) |  |  |  |
|  |  |  |  | 1 | 2 | 3 | 4 | 5 | 6 |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \\ & \hline \end{aligned}$ |  |  | (B) | $\begin{gathered} \text { (C) } 11-20 \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \\ & \hline \end{aligned}$ |  |  |  | $\begin{aligned} & \text { (B) } \\ & 6-10 \end{aligned}$ |  | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ |  | GN |
| P | H | T | 74409111615 | x | x |  |  |  |  | c | A902 | CIRCUIT CARD ASSEMBLY: <br> 58189: A53725-001 |  | EA |  | 2 | 1 | 2 | 3 | 1 | 2 |  | 3 |  | 3 | $\begin{aligned} & -15 \\ & 4-8 \end{aligned}$ | 8 |
| X1 | D |  |  | x | x |  |  |  |  | D | A903 | PRINTED CIRCUIT BOARD: <br> 58189: A53726-001 | EA |  | 2 |  |  |  |  |  |  |  |  | -15 $5-5$ |  |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A904 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z1 |
|  |  |  | 59627911082 | X | x |  |  |  |  | D | A905 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-5$ | Z2 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A906 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z3 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A907 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r} -15 \\ 5-5 \end{array}$ | Z4 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A908 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z9 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A909 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z10 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A910 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z11 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A911 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z12 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (6) |  |  |  | ${ }^{(8)}$ <br> 45 DAY AREA RESUPPLY ALLOW. bASED ON NO. EQUIP. SUPPORTED |  |  | $\begin{array}{\|c\|} \hline \text { (9) } \\ 1 \mathrm{YR} . \\ \text { ALW. } \\ \text { PER } \\ 100 \\ \text { EQUUP } \\ \text { CNTG } \\ \text { CY PL. } \\ \hline \end{array}$ | (10) <br> DEPOT <br> MAINT <br> ALW. <br> PRR <br> 100 <br> EQUIP. | $\stackrel{(11)}{\text { ILLUSTRATIONS }}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | (C) <br> REC <br> code | $\stackrel{(2)}{\text { FEDERAL }}$ STOCK NUMBER | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { INC } \\ & \text { IN } \end{aligned}$ |  |  |  | (A) | (B) |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & (\mathbf{A}) \\ & 1-5 \end{aligned}$ | (B) | $\begin{gathered} \text { 11-20 } \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ |  |  |  | $\begin{array}{\|c} \text { (B) } \\ 6-10 \end{array}$ |  | $\left(\begin{array}{c} \left(\begin{array}{c} 1-20 \end{array}\right) \end{array}\right.$ |  | DESIGN |
|  |  |  | 59627911082 | X | x |  |  |  |  | D | A912 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 |  | EA |  | REF |  |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z17 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A913 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z18 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A914 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-5$ | Z19 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A915 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-5$ | Z20 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A916 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-5 \end{gathered}$ | Z25 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A917 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z26 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A918 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z27 |
|  |  |  | 59627911082 | X | $x$ |  |  |  |  | D | A919 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z28 |
|  |  |  | 74409111615 | x | x |  |  |  |  | c | A920 | CIRCUIT, CARD ASSEMBLY: <br> SAME AS A902 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 4-8 \end{aligned}$ | 8 |
|  |  |  |  |  | x |  |  |  |  | D | A921 | PRINTED CIRCUIT BOARD: <br> SAME AS A903 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ |  |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  | (5) <br> QTy | (6) <br> QTY <br> INC <br> IN UNIT | (30 DAYS) SITE STOCKAGE ALLOWANCE |  |  | (8)45 DAY AREARESUPPLY ALLOW.BASED ON NO.EQUIP. SUPPORTED |  |  | (9) <br> 1 YR <br> ALW. <br> PER <br> 100 <br> EQUP <br> CNTG <br> CY PL. | (10) <br> DEPOT <br> MANT <br> ALW. <br> PRR <br> 100 <br> EQUIP. | (11) iLLUSTRATIONS |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | $\begin{array}{\|c\|c} \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | (2)FEDERALSTOCKNUMBER | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { IN } \\ & \text { UN } \end{aligned}$ |  |  |  |  | (A) |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \\ & \hline \end{aligned}$ |  | (B) | $\begin{gathered} \text { (C) (C) } \\ 11-20 \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \\ & \hline \end{aligned}$ |  |  |  | $\begin{aligned} & \text { (B) } \\ & 6-10 \end{aligned}$ |  | $\begin{gathered} \text { (C) } \\ \hline 11-20 \\ \hline \end{gathered}$ |  | DESIGN |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A922 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 |  | EA |  | REF |  |  |  |  |  |  |  |  |  | -15 $5-5$ | Z1 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A923 | INTEGRATED CIRCUIT, LOGIC GATE: <br> SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z2 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A924 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z3 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A925 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z4 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A926 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-5 \end{gathered}$ | Z9 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A927 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z10 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A928 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z11 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A929 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r} -15 \\ 5-5 \end{array}$ | Z12 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A930 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z17 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A931 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{array}{r} -15 \\ 5-5 \end{array}$ | Z18 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (6) | $\qquad$ |  |  | (8)45 DAY AREARESUPPLY ALLOW.BASED ON NO.EQUIP. SUPPORTED |  |  | (9) <br> 1 YR. <br> ALW. <br> PER <br> 100 <br> EQUIP <br> COTG <br> CY PL. |  | $\stackrel{(11)}{\text { illustrations }}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} \text { (A) } \\ \text { SRCE } \\ \text { CD } \end{gathered}$ | (B) <br> MNTC DC | $\begin{array}{\|c\|} \hline \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ |  | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  | $\left\lvert\, \begin{gathered} \text { INC } \\ \text { IN } \\ \text { UNIT } \end{gathered}\right.$ |  |  |  | (A) FIGURE | (B) ITEM NO. |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ | (B-10 | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ |  |  |  | $\begin{array}{\|c\|c\|} (\text { B }) \\ \text { (B) } \end{array}$ |  | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ |  | DESIGN |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A932 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 |  | EA |  | REF |  |  |  |  |  |  |  |  |  | $\begin{array}{r} -15 \\ 5-5 \end{array}$ | Z19 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | 933 | INTEGRATED CIRCUIT, LOGIC GATE: <br> SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z20 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A934 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-5 \end{aligned}$ | Z25 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A935 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-5$ | Z26 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A936 | INTEGRATED CIRCUIT, LOGIC GATE: SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-5 \end{gathered}$ | Z27 |
|  |  |  | 59627911082 | x | x |  |  |  |  | D | A937 | INTEGRATED CIRCUIT, LOGIC GATE: <br> SAME AS A842 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-5 \end{gathered}$ | Z28 |
| P | H | T | 74409352376 | x | x |  |  |  |  | C | A938 | CIRCUIT, CARD ASSEMBLY: <br> 58189: A65205-001 | EA |  | 1 | 1 | 2 | 3 | 1 | 2 | 3 |  | 3 | $\begin{aligned} & -15 \\ & 4-8 \end{aligned}$ | 4 |
| X1 | D |  |  | x | x |  |  |  |  | D | A939 | PRINTED CIRCUIT BOARD: <br> 58189: A65206-001 | EA |  | 1 |  |  |  |  |  |  |  |  | -15 $5-6$ |  |
| P | D |  | 59107028057 | x | x |  |  |  |  | D | A940 | CAPACITOR, FIXED, MICA: 81349: CM05F331J03 | EA |  | 9 |  |  |  |  |  |  |  | 45 | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | C1 |
|  |  |  | 59107028057 | x | x |  |  |  |  | D | A941 | CAPACITOR, FDIXED, MICA: SAME AS A940 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | C2 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (6) | (7) 30 DAYS SITE STOCKAGE ALLOWANCE |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW. BASED ON NO. EQUIP. SUPPORTED |  |  | (9) <br> 1 YR. <br> ALW. <br> PER <br> 100 <br> EQUIP <br> CNTG <br> CY PL. | (10) <br> DEPOT <br> MANT <br> ALW. <br> PRR <br> 100 <br> EQUIP. | (11) ILLUSTRATIONS |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC DC | $\begin{array}{\|c\|c} \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | $\begin{aligned} & \text { (2) } \\ & \text { FEDERAL } \\ & \text { STOCK } \\ & \text { NUMBER } \end{aligned}$ | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  | $\left\lvert\, \begin{gathered} \text { INC } \\ \text { IN } \\ \text { UNIT } \end{gathered}\right.$ |  |  |  | (A) | (B) |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ | (B-10 | $\begin{gathered} \text { (C) (C) } \\ \hline 120 \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \\ & \hline \end{aligned}$ |  |  |  | $\begin{aligned} & \text { (B) } \\ & 6-10 \end{aligned}$ |  | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ |  | DESIGN |
| P | D |  | 59056819969 | X | x |  |  |  |  | D | A952 | RESISTOR, FIXED, COMPOSITION: <br> 81349: RC07GF332J |  | EA |  | 9 |  |  |  |  |  |  |  |  | 27 | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | R1 |
|  |  |  | 59056819969 | x | x |  |  |  |  | D | A953 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A952 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R11 |
|  |  |  | 59056819969 | x | x |  |  |  |  | D | A954 | RESISTOR, FDIXED, COMPOSITION: <br> SAME AS A952 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R21 |
|  |  |  | 59056819969 | x | x |  |  |  |  | D | A955 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A952 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R31 |
|  |  |  | 59056819969 | x | x |  |  |  |  | D | A956 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A952 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R41 |
|  |  |  | 59056819969 | x | x |  |  |  |  | D | A957 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A952 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R51 |
|  |  |  | 59056819969 | x | x |  |  |  |  | D | A958 | RESISTOR, FLXED, COMPOSITION: <br> SAME AS A952 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R61 |
|  |  |  | 59056819969 | x | x |  |  |  |  | D | A959 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A952 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R71 |
|  |  |  | 59056819969 | . x | x |  |  |  |  | D | A960 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A952 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R81 |
| P | D |  | 59056869997 | x | x |  |  |  |  | D | A961 | RESISTOR, FIXED, COMPOSITION: 81349: RC07GF682J | EA |  | 9 |  |  |  |  |  |  |  | 27 | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R2 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (6) |  |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW. bASED ON NO EQUIP. SUPPORTED |  |  | $\begin{array}{\|c\|} \hline \text { (9) } \\ 1 \mathrm{YR} . \\ \text { ALW. } \\ \text { PER } \\ 100 \\ \text { EQUUP } \\ \text { CNTG } \\ \text { CY PL. } \\ \hline \end{array}$ | (10) <br> DEPOT <br> MANT <br> ALW. <br> PRR <br> 100 <br> EQUIP. | ${ }_{\text {ILLUSTRATIONS }}^{(11)}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | $\begin{array}{\|c\|c} \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | $\stackrel{(2)}{\text { FEDERAL }}$ STOCK NUMBER | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  | INC IN |  |  |  | (A) | (B) |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & (\mathbf{A}) \\ & 1-5 \end{aligned}$ | (B) | $\begin{gathered} \text { 11-20 } \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ |  |  |  | $\begin{array}{\|c} \text { (B) } \\ 6-10 \end{array}$ |  | $\begin{aligned} & \text { (C) } 11-20 \end{aligned}$ |  | DESIGN |
|  |  |  | 59056869997 | X | x |  |  |  |  | D | A962 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A961 |  | EA |  | REF |  |  |  |  |  |  |  |  |  | -15 $5-6$ | R12 |
|  |  |  | 59056869997 | x | x |  |  |  |  | D | A963 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A961 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | R22 |
|  |  |  | 59056869997 | x | x |  |  |  |  | D | A964 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A961 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | R32 |
|  |  |  | 59056869997 | x | x |  |  |  |  | D | A965 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A961 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | R42 |
|  |  |  | 59056869997 | x | x |  |  |  |  | D | A966 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A961 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | R52 |
|  |  |  | 59056869997 | x | x |  |  |  |  | D | A967 | RESISTOR, FIXED, COMPOSITION: SAME AS A961 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R62 |
|  |  |  | 59056869997 | X | $x$ |  |  |  |  | D | A968 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A961 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R72 |
|  |  |  | 59056869997 | x | x |  |  |  |  | D | A969 | RESTSTOR, FIXED, COMPOSITION: <br> SAME AS A961 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R82 |
| P | D |  | 59058000179 | x | x |  |  |  |  | D | A970 | RESISTOR, FIXED, COMPOSITION: 81349: RC07GF563J | EA |  | 10 |  |  |  |  |  |  |  | 30 | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R3 |
|  |  |  | 59058000179 | x | x |  |  |  |  | D | A971 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A970 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | R13 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (6) |  |  |  | ${ }^{(8)}$ <br> 45 DAY AREA RESUPPLY ALLOW. bASED ON NO. EQUIP. SUPPORTED |  |  | $\begin{array}{\|c\|} \hline \text { (9) } \\ \text { 1 YR. } \\ \text { ALW. } \\ \text { PER } \\ \text { 100 } \\ \text { EQUIP } \\ \text { CNTG } \\ \text { CY PL. } \\ \hline \end{array}$ | (10) <br> DEPOT <br> MANT <br> ALW. <br> PRR <br> 100 <br> EQUIP. | $\stackrel{(11)}{\text { ILLUSTRATIONS }}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | $\begin{array}{\|c\|c} \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | $\stackrel{(2)}{\text { FEDERAL }}$ STOCK NUMBER | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { INC } \\ & \text { IN } \end{aligned}$ |  |  |  | (A) | (B) |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & (\mathbf{A}) \\ & 1-5 \end{aligned}$ | (B) | $\begin{gathered} \text { 11-20 } \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ |  |  |  | $\begin{array}{\|c} \text { (B) } \\ 6-10 \end{array}$ |  | $\left\lvert\, \begin{gathered} \text { (C) } \\ 11-20 \end{gathered}\right.$ |  | DESIGN |
|  |  |  | 59058000179 | X | x |  |  |  |  | D | A972 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A970 |  | EA |  | REF |  |  |  |  |  |  |  |  |  | -15 $5-6$ | R23 |
|  |  |  | 59058000179 | x | x |  |  |  |  | D | A973 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A970 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | R33 |
|  |  |  | 59058000179 | x | x |  |  |  |  | D | A974 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A970 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | R43 |
|  |  |  | 59058000179 | x | x |  |  |  |  | D | A975 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS P970 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | R53 |
|  |  |  | 59058000179 | x | x |  |  |  |  | D | A976 | RESISTOR.FIXED, COMPOSITION: <br> SAME AS A970 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | R63 |
|  |  |  | 59058000179 | x | x |  |  |  |  | D | A977 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A970 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R73 |
|  |  |  | 59058000179 | x | x |  |  |  |  | D | A978 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A970 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R83 |
| P | D |  | 59051858510 | x | x |  |  |  |  | D | A979 | RESISTOR, FIXED, COMPOSITION: 81349: RC07GF103J | EA |  | 22 |  |  |  |  |  |  |  | 66 | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R4 |
|  |  |  | 59051858510 | x | $x$ |  |  |  |  | D | A980 | RESISTOR, FIXED, COMPOSITION: SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R7 |
|  |  |  | 5905185810 | x | x |  |  |  |  | D | A981 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | R14 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  | (4) <br> UNIT | (5) <br> QTY <br> INC <br> IN <br> UN <br> PK | (6) <br> QTY <br> INC <br> IN UNIT | (7) (30 DAYS) SITE STOCKAGE ALLOWANCE |  |  | (8) 45 DAY AREA RESUPPLY ALLOW. BASED ON NO. EQUIP. SUPPORTED |  |  | (9) <br> 1 YR. <br> ALW. <br> PER <br> 100 <br> EQUIP <br> CNTG <br> CY PL. | (10) <br> DEPOT <br> MANT <br> ALW. <br> PRR <br> 100 <br> EQUIP. | (11) illustrations |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) (C) <br> MNTC REC <br> DC CODE |  | $\stackrel{(2)}{\text { FEDERAL }}$ STOCK NUMBER | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  | ISSUE |  |  |  |  |  | $\stackrel{\text { (A) }}{\text { FIGURE }}$ | (B) ITEM NO. |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \\ & \hline \end{aligned}$ |  |  | (B) | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \\ & \hline \end{aligned}$ |  |  |  | $\begin{aligned} & \text { (B) } \\ & 6-10 \end{aligned}$ |  | $\begin{gathered} \text { (C) } \\ \hline 11-20 \\ \hline \end{gathered}$ |  | DESIGN |
|  |  |  |  | 59051858510 | x | x |  |  |  |  | D | A982 | RESISTOR, FIXED, COMPOSITION: SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  |  | -15 $5-6$ | R17 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A983 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R24 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A984 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R27 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A985 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R34 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A986 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R37 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A987 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R44 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A988 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R47 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A989 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R54 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A990 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R57 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A991 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & -6 \end{aligned}$ | R64 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (6) | $\qquad$ |  |  | (8)45 DAY AREARESUPPLY ALLOW.BASED ON NO.EQUIP. SUPPORTED |  |  | (9) <br> 1 YR. <br> ALW. <br> PER <br> 100 <br> EQUIP <br> COTG <br> CY PL. | (10) <br> DEPOT <br> MANT <br> ALW. <br> PER <br> 100 <br> EOUIP. | $\stackrel{(11)}{\text { ILLUSTRATIONS }}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC DC | $\begin{array}{\|c\|} \hline \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ |  | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { INC } \\ & \text { IN } \\ & \text { UNIT } \end{aligned}$ |  |  |  |  | (B) ITEM NO. |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ | $\begin{gathered} (\mathrm{B}) \\ 6-10 \end{gathered}$ | (C) (C) | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ |  |  |  | $\begin{array}{\|c\|c\|} \hline \text { (B) } \\ 6 \text { ( } \end{array}$ |  | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ |  | DESIGN |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A992 | RESISTOR, FIXED, COMPOSITION: SAME AS A979 |  | EA |  | REF |  |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R67 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A993 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | R74 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A994 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R77 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A995 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS P. 979 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | R84 |
|  |  |  | 59051858510 | x | x |  |  |  |  | D | A996 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A979 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-G \end{aligned}$ | R87 |
| P | D |  | 59056863903 | x | $x$ |  |  |  |  | D | A997 | RESISTOR, FIXED, COMPOSITION: <br> 81349: RC07GF333J | EA |  | 9 |  |  |  |  |  |  |  | 27 | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | R5 |
|  |  |  | 59056863903 | x | x |  |  |  |  | D | A998 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A997 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R15 |
|  |  |  | 59056863903 | x | x |  |  |  |  | D | A999 | RESISTOR, FIXED, COMPOSITION: SAME AS A997 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R25 |
|  |  |  | 59056863903 | x | x |  |  |  |  | D | B001 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A997 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R35 |
|  |  |  | 59056863903 | x | x |  |  |  |  | D | B002 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A997 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R45 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  | (4) | $\begin{aligned} & \text { (5) } \\ & \text { QTY } \\ & \text { INC } \\ & \text { IN } \\ & \text { UN } \\ & \text { PK } \end{aligned}$ | (6) <br> QTY <br> INC <br> IN UNIT | (30 DAYS SITE STOCKAGE ALLOWANCE |  |  | (8)45 DAY AREARESUPPLY ALLOW.BASED ON NO.EQUIP. SUPPORTED |  |  | (9) <br> 1 YR <br> ALW. <br> PER <br> 100 <br> EQUP <br> CNTG <br> CY PL. | (10) <br> DEPOT MAINT ALW. 100 EQUIP. | (11) illustrations |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | $\begin{array}{\|c\|c} \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | (2)FEDERALSTOCKNUMBER | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  | ISSUE |  |  |  |  |  | (A) | (B) |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & (\mathbf{A}) \\ & 1-5 \end{aligned}$ | (B-10 | $\begin{gathered} \text { (C) (C) } \\ \hline 120 \end{gathered}$ |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \text { (B) } \\ & 6-10 \end{aligned}$ | $\begin{array}{\|c} \text { (C) } \\ 11-20 \\ \hline \end{array}$ |  | DESIGN |
| P | D |  | 59056863903 | x | x |  |  |  |  | D | B003 | RESISTOR, FIXED, COMPOSITION: SAME AS A997 | EA |  | REF |  |  |  |  |  |  |  |  |  | -15 $5-6$ | R55 |
|  |  |  | 59056863903 | x | x |  |  |  |  | D | B004 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A997 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R65 |
|  |  |  | 59056863903 | x | x |  |  |  |  | D | B005 | RESISTOR, FIXED, COMPOSITION: SAME AS A997 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R75 |
|  |  |  | 59056863903 | x | x |  |  |  |  | D | 8006 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS A997 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R85 |
|  |  |  | 59058016998 | x | x |  |  |  |  | D | B007 | RESISTOR, FIXED, COMPOSITION: 81349: RC07GF621J | EA |  | 9 |  |  |  |  |  |  |  | 27 | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | R6 |
|  |  |  | 59058016998 | x | x |  |  |  |  | D | B008 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B007 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R16 |
|  |  |  | 59058016998 | x | x |  |  |  |  | D | B009 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS 8007 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R26 |
|  |  |  | 59058016998 | x | x |  |  |  |  | D | B010 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B007 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R36 |
|  |  |  | 59058016998 | x | x |  |  |  |  | D | B011 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B007 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R46 |
|  |  |  | 59058016998 | x | x |  |  |  |  | D | B012 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B007 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R56 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{array}{\|l\|} \text { (6) } \\ \text { OTY } \\ \text { INC } \\ \text { IN } \\ \text { UNIT } \end{array}$ |  |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW. BASED ON NO. EQUIP. SUPPORTED |  |  | $\begin{array}{\|c\|} \hline \text { (9) } \\ 1 \mathrm{YR} . \\ \text { ALW. } \\ \text { PER } \\ \text { 100 } \\ \text { EQUPP } \\ \text { CNTG } \\ \text { CY PL. } \\ \hline \end{array}$ | (10) <br> DEPOT <br> MAINT <br> ALW. <br> PRR <br> 100 <br> EQUIP. | $\text { ILLuStRATIONS }_{(11)}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | $\begin{gathered} \text { (C) } \\ \text { REC } \\ \text { CODE } \end{gathered}$ | ${ }^{(2)}$ | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (A) | (B) |  |  |
|  |  |  | NUMBER |  |  |  |  |  |  |  |  |  | $\begin{aligned} & (\mathbf{A}) \\ & 1-5 \end{aligned}$ |  |  | (B) | $\begin{gathered} \text { 11-20 } \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ |  |  |  | $\begin{array}{\|c} \text { (B) } \\ 6-10 \end{array}$ |  | $\begin{aligned} & \text { (C) } 11-20 \end{aligned}$ |  | DESIGN |
|  |  |  | 59051955571 | X | x |  |  |  |  | D | B023 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B016 |  | EA |  | REF |  |  |  |  |  |  |  |  |  | -15 $5-6$ | R39 |
|  |  |  | 59051955571 | x | x |  |  |  |  | D | B024 | RESISTOR, FIXED, COMPPOSITION: <br> SAME AS B016 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | R48 |
|  |  |  | 59051955571 | x | x |  |  |  |  | D | B025 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B016 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | R49 |
|  |  |  | 59051955571 | x | x |  |  |  |  | D | B026 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B016 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | R58 |
|  |  |  | 59051955571 | x | x |  |  |  |  | D | B027 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B016 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | R59 |
|  |  |  | 59051955571 | x | x |  |  |  |  | D | B028 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B016 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R68 |
|  |  |  | 59051955571 | x | $x$ |  |  |  |  | D | B029 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B016 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R69 |
|  |  |  | 59051955571 | x | x |  |  |  |  | D | B030 | RESISTOR, FXED, COMPOSITION: <br> SAME AS B016 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R78 |
|  |  |  | 59051955571 | x | x |  |  |  |  | D | B031 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B016 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R79 |
|  |  |  | 59051955571 | x | x |  |  |  |  | D | B032 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS 8016 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | R88 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (6) | (7) 30 DAYS SITE STOCKAGE ALLOWANCE |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW. BASED ON NO. EQUIP. SUPPORTED |  |  | (9) <br> 1 YR. <br> ALW. <br> PER <br> 100 <br> EQUIP <br> CNTG <br> CY PL. | (10) <br> DEPOT <br> MANT <br> ALW. <br> PRR <br> 100 <br> EQUIP. | ${ }_{\text {ILLUSTRATIONS }}^{(11)}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | $\begin{array}{\|c\|} \hline \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | $\begin{aligned} & \text { (2) } \\ & \text { FEDERAL } \\ & \text { STOCK } \\ & \text { NUMBER } \end{aligned}$ | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  | $\left\lvert\, \begin{gathered} \text { INC } \\ \text { IN } \\ \text { UNIT } \end{gathered}\right.$ |  |  |  | (A) | (B) |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ | (B-10 | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \\ & \hline \end{aligned}$ |  |  |  | $\begin{aligned} & \text { (B) } \\ & 6-10 \end{aligned}$ |  | $\begin{array}{\|c} \text { (C) } \\ 11-20 \\ \hline \end{array}$ |  | DESIGN |
| P | D |  | 59051955571 | x | x |  |  |  |  | D | в033 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B016 |  | EA |  | REF |  |  |  |  |  |  |  |  |  | -15 $5-6$ | R89 |
|  |  |  | 59056910195 | x | x |  |  |  |  | D | B034 | RESISTOR, FIXED, COMPOSITION: <br> 81349: RC07GF562J | EA |  | 9 |  |  |  |  |  |  |  | 27 | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | R10 |
|  |  |  | 59056910195 | x | x |  |  |  |  | D | B035 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B034 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R20 |
|  |  |  | 59056910195 | x | x |  |  |  |  | D | B036 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B034 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R30 |
|  |  |  | 59056910195 | x | x |  |  |  |  | D | B037 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B034 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | R40 |
|  |  |  | 59056910195 | x | x |  |  |  |  | D | B038 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B034 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R50 |
|  |  |  | 59056910195 | x | x |  |  |  |  | D | B039 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B034 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R60 |
|  |  |  | 59056910195 | x | x |  |  |  |  | D | B040 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B034 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R70 |
|  |  |  | 59056910195 | x | x |  |  |  |  | D | B041 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS 3034 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R80 |
|  |  |  | 59056910195 | x | x |  |  |  |  | D | B042 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS 8034 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R90 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{array}{\|c} \text { (6) } \\ \text { QTY } \\ \text { INC } \\ \text { IN } \\ \text { UNIT } \end{array}$ | (7) 30 DAYS SITE STOCKAGE ALLOWANCE |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW. BASED ON NO. EQUIP. SUPPORTED |  |  | (9) <br> 1 YR. <br> ALW. <br> PER <br> 100 <br> EQUIP <br> CNTG <br> CY PL. | (10) <br> DEPOT <br> MANT <br> ALW. <br> PRR <br> 100 <br> EQUIP. | ${ }_{\text {ILLUSTRATIONS }}^{(11)}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | $\begin{array}{\|c\|c} \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ |  | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (A) Figure NUMBER | (B) ITEM NO. OR REF DESIGN |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $P$ <br>  <br>  | D |  | 59052792627 | x | x |  |  |  |  | D | B043 | RESISTOR, FIXED, COMPOSITION: <br> 81349: RC42GF750J | EA |  | 2 |  |  |  |  |  |  |  | 6 | -15 $5-6$ | R9 |
|  |  |  | 59052792627 | x | x |  |  |  |  | D | B044 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS 8043 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | R92 |
|  | D |  | 59618140768 | x | x |  |  |  |  | D | B045 | SEMI-CONDUCTOR DEVICE DIODE: <br> 81350: JAN1N3064 | EA |  | 28 |  |  |  |  |  |  |  | 84 | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR1 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B046 | SEMI-CONDUCTOR DEVICE DIODE: <br> SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR2 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B047 | SEMI-CONDUCTOR DEVICE DIODE: SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR3 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B048 | SEMI-CONDUCTOR DEVICE, DIODE: <br> SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR4 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B049 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR5 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B050 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR6 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B051 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR7 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B052 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR8 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  | (5) <br> QTy | (6) <br> QTY <br> INC <br> IN UNIT | (30 DAYS SITE STOCKAGE ALLOWANCE |  |  | (8)45 DAY AREARESUPPLY ALLOW.BASED ON NO.EQUIP. SUPPORTED |  |  | (9) <br> 1 YR <br> ALW. <br> PER <br> 100 <br> EQUP <br> CNTG <br> CY PL. | (10) <br> DEPOT <br> MAINT <br> ALW. <br> PER <br> 100 <br> EQUIP. | (11) iLLUSTRATIONS |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | $\begin{array}{\|c\|} \hline \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | $\stackrel{(2)}{\text { FEDERAL }}$ STOCK NUMBER | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { IN } \\ & \text { UN } \end{aligned}$ |  |  |  |  | (A) |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ |  | (B) | $\begin{gathered} \text { (C) (C) } \\ 11-20 \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \\ & \hline \end{aligned}$ |  |  |  | $\begin{aligned} & \text { (B) } \\ & 6-10 \end{aligned}$ |  | $\begin{gathered} \text { (C) } \\ \hline 11-20 \\ \hline \end{gathered}$ |  | DESIGN |
|  |  |  | 59618140768 | x | x |  |  |  |  |  | B053 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B045 |  | EA |  | REF |  |  |  |  |  |  |  |  |  | -15 $5-6$ | CR9 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B054 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR10 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B055 | SEMI-CONDUCTOR DEVICE, DIODE: <br> SAME AS 8045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR11 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B056 | SEMI-CONDUCTOR DEVICE, DIODE: <br> SAME AS 8045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR12 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B057 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR13 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B058 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR14 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B059 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR15 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B060 | SEMI-CONDUCTOR DEVICE, DIODE: <br> SAME AS 8045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | CR16 |
|  |  |  | 59618140768 | X | X |  |  |  |  | D | B061 | SEMI-CONDUCTOR DEVICE , DIODE: SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | CR17 |
|  |  |  | 59618140768 | x | x |  |  |  |  | D | B062 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B045 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | CR18 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  | SITE, AREA RESUPPLY,    <br> AINTENANCE   $\quad$ (4)(5) <br> UNIT <br> OTY <br> OF <br>  <br>  <br>  <br>  <br>  <br>  <br>  <br>  <br>  <br> DESCRIPTION | (6) | $\qquad$ |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW. BASED ON NO. EQUIP. SUPPORTED |  |  | (9) <br> 1 YR. <br> ALW. <br> PER <br> 100 <br> EQUP <br> CNTG <br> CY PL. | (10)DEPOTMANTALW.PER100EOUIP. | $\stackrel{(11)}{\text { illustrations }}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC DC | $\begin{array}{\|c\|} \hline \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | $\stackrel{(2)}{\text { FEDERAL }}$ STOCK NUMBER | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  | $\left\lvert\, \begin{gathered} \text { INC } \\ \text { IN } \\ \text { UNIT } \end{gathered}\right.$ |  |  |  |  | (B) ITEM NO. |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ | $\begin{gathered} (B) \\ 6-10 \end{gathered}$ | $\begin{gathered} \text { (C) (C) } \\ 11-20 \end{gathered}$ | $\begin{aligned} & (\mathrm{A}) \\ & 1-5 \end{aligned}$ |  |  |  | $\begin{aligned} & \text { (B) } \\ & 6-10 \end{aligned}$ |  | $\begin{array}{\|c} \text { (C) } \\ 11-20 \end{array}$ |  | GN |
| P | D |  | 59610680687 | x | x |  |  |  |  | D | B063 | SEMI-CONDUCTOR DEVICE, DIODE: 81350: JAN1N3828A |  | EA |  | 3 |  |  |  |  |  |  |  |  | 9 | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | VR1 |
|  |  |  | 59610680687 | x | x |  |  |  |  | D | B064 | SEMI-CONDUCTOR DEVICE, DIODE: <br> SAME AS B063 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | VR2 |
| P | D |  | 59610507499 | x | x |  |  |  |  | D | B065 | TRANSISTOR: 81350: JAN2N2219 | EA |  | 32 |  |  |  |  |  |  |  | 160 | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | Q1 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B066 | TRANSISTOR: SAME AS B065 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | Q3 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B067 | TRANSISTOR: SAME AS B065 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | Q5 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B068 | TRANSISTOR: <br> SAME AS 8065 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | Q7 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B069 | TRANSISTOR: SAME AS B065 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | Q9 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B070 | TRANSISTOR: SAME AS 8065 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | Q11 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B071 | TRANSISTOR: SAME AS B065 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | Q13 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B072 | TRANSISTOR: <br> SAME AS B065 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-6 \end{gathered}$ | Q15 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B073 | TRANSISTOR: <br> SAME AS 8065 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | Q17 |
|  |  |  | 59610507499 |  | x |  |  |  |  | D | B074 | TRANSISTOR: SAME AS B065 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-6 \end{aligned}$ | Q19 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  | SITE, AREA RESUPPLY,   (4) <br> AINTENANCE    (5) | (6) |  |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW. BASED ON NO. EQUIP. SUPPORTED |  |  | $\begin{array}{\|c\|} \hline \text { (9) } \\ 1 \text { YR. } \\ \text { ALW. } \\ \text { PER } \\ 100 \\ \text { EQUIP } \\ \text { CNGG } \\ \text { CY PL. } \\ \hline \end{array}$ | (10) <br> DEPOT <br> MAINT <br> ALW. <br> PRR <br> 100 <br> EQUIP. | $\stackrel{(11)}{ }_{\text {ILLUSTRATIONS }}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | $\begin{array}{\|c\|c} \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | $\stackrel{(2)}{\text { FEDERAL }}$ STOCK NUMBER | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  | INC IN |  |  |  | (A) | (B) |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ | (B) | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ |  |  |  | $\begin{aligned} & \text { (B) } \\ & 6-10 \end{aligned}$ |  | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ |  | IGN |
|  |  |  | 59618804779 | x | x |  |  |  |  | D | 8099 | TRANSISTOR; SAME AS B083 |  | EA |  | REF |  |  |  |  |  |  |  |  |  | -15 $5-6$ | Q34 |
|  |  |  | 59618804779 | X | x |  |  |  |  | D | B100 | TRANSISTOR: SAME AS B083 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | Q36 |
|  |  |  | 59709564972 | x | x |  |  |  |  | D | B101 | INSULATOR, DISK SAME AS A209C | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-6$ | H1 |
| A | H | T |  | X | x |  |  |  |  | C | B101A | CIRCUIT CARD ASSEMBLY: <br> 58189: A65227-001 | EA |  | 1 |  |  |  |  |  |  |  |  | -15 $4-8$ | 4.1 |
| X1 | D |  |  | x | x |  |  |  |  | D | B101B | PRINTED CIRCUIT BOARD: <br> 58189: A65228-001 | EA |  | 1 |  |  |  |  |  |  |  |  | -15 $5-8.2$ |  |
| P | D |  | 74401343719 | x | x |  |  |  |  | D | B101C | ELECTRONIC COMPONENT ASSEMBLY: <br> 58189: T00023-004 | EA |  | 9 |  |  |  |  |  |  |  | 27 | $\begin{gathered} -15 \\ 5-8.2 \end{gathered}$ | Z1 |
|  |  |  | 74401343719 | x | x |  |  |  |  | D | B101D | ELECTRONIC COMPONENT ASSEMBLY: <br> SAME AS B101C | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-8.2 \end{gathered}$ | Z2 |
|  |  |  | 74401343719 | X | x |  |  |  |  | D | B101E | ELECTRONIC COMPONENT ASSEMBLY: <br> SAME AS B101C | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-8.2 \end{gathered}$ | Z3 |
|  |  |  | 74401343719 | x | x |  |  |  |  | D | B101F | ELECTRONIC COMPONENT ASSEMBLY: <br> SAME AS B101C | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-8.2 \end{gathered}$ | Z4 |
|  |  |  | 74401343719 | x | x |  |  |  |  | D | B101G | ELECTRONIC COMPONENT ASSEMBLY: <br> SAME AS B101C | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-8.2 \end{gathered}$ | Z5 |
|  |  |  | 74401343719 | x | x |  |  |  |  | D | B101H | ELECTRONIC COMPONENT ASSEMBLY: <br> SAME AS B101C | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{gathered} -15 \\ 5-8.2 \end{gathered}$ | Z6 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  | SITE, AREA RESUPPLY,    <br> AINTENANCE   $\quad$ (4)(5) <br> UNIT <br> OTY <br> OF <br>  <br>  <br>  <br>  <br>  <br>  <br>  <br>  <br>  <br> DESCRIPTION | (6) | $\qquad$ |  |  |  |  |  | (9) <br> 1 YR. <br> ALW. <br> PER <br> 100 <br> EOUIP <br> CNTG <br> CY PL. | $\begin{array}{\|c\|} \hline \text { (10) } \\ \text { DEPOT } \\ \text { MAINT } \\ \text { ALW. } \\ \text { PER } \\ 100 \\ \text { EQUIP. } \end{array}$ | $\stackrel{(11)}{\text { ILLUSTRATIONS }}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC <br> DC | $\begin{array}{\|c\|} \hline \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | $\stackrel{(2)}{\text { FEDERAL }}$ STOCK NUMBER | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  | $\begin{array}{\|l\|l} \text { INC } \\ \text { IN } \end{array}$ |  |  |  | $\stackrel{\text { (A) }}{\text { Fig }}$ | (B) |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & (\mathrm{A}) \\ & 1-5 \end{aligned}$ | $\begin{gathered} (B) \\ 6-10 \end{gathered}$ | $\begin{gathered} \text { (C) } \\ \text { (C) } \end{gathered}$ | $\begin{aligned} & (\mathrm{A}) \\ & 1-5 \end{aligned}$ |  |  |  | $\begin{aligned} & \text { (B) } \\ & 6-10 \end{aligned}$ |  | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ |  | , |
| P | D |  | 59109960666 | x | x |  |  |  |  | D | B110 | CAPACITOR, FIXED, ELECTROLYTIC: 81349: CS13BC227M |  | EA |  | 1 |  |  |  |  |  |  |  |  | 5 | $\begin{aligned} & -15 \\ & 5-7 \end{aligned}$ | C6 |
| P | D |  | 59056863368 | x | x |  |  |  |  | D | B111 | RESISTOR, FIXED, COMPOSITION: 81349: RC07GF203J | EA |  | 2 |  |  |  |  |  |  |  | 3 | $\begin{aligned} & -15 \\ & 5-7 \end{aligned}$ | R1 |
| P | D |  | 59052291971 | x | x |  |  |  |  | D | B112 | RESISTOR, FIXED, COMPOSITION: 81349: RC20GF822J | EA |  | 1 |  |  |  |  |  |  |  | 3 | $\begin{aligned} & -15 \\ & 5-7 \end{aligned}$ | R2 |
| P | D |  | 59057235251 | x | x |  |  |  |  | D | B113 | RESISTOR, FIXED, COMPOSITION: 81349: RC:07GF222J | EA |  | 1 |  |  |  |  |  |  |  | 3 | $\begin{aligned} & -15 \\ & 5-7 \end{aligned}$ | R3 |
| P | D |  | 59056863798 | x | x |  |  |  |  | D | B114 | RESISTOR, FIXED, COMPOSITION: 81349: RC07GF272J | EA |  | 5 |  |  |  |  |  |  |  | 15 | $\begin{gathered} -15 \\ 5-7 \end{gathered}$ | R4 |
| P | D |  | 59056816462 | x | x |  |  |  |  | D | 8115 | RESISTOR, FIXED, COMPOSITION: 81349: RC07GF102J | EA |  | 16 |  |  |  |  |  |  |  | 48 | $\begin{aligned} & -15 \\ & 5-7 \end{aligned}$ | R5 |
|  |  |  | 59056816462 | x | x |  |  |  |  | D | 8116 | RESISTOR, FIXED, COMPOSITION: SAME AS B115 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-7 \end{aligned}$ | R22 |
|  |  |  | 59056816462 | x | x |  |  |  |  | D | 8117 | RESISTOR, FIXED, COMPOSITION: SAME AS B115 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-7 \end{aligned}$ | R23 |
| P | D |  | 59056832241 | x | x |  |  |  |  | D | B118 | RESISTOR, FIXED. COMPOSITION: 81349: RC07GF512J | EA |  | 1 |  |  |  |  |  |  |  | 3 | $\begin{aligned} & -15 \\ & 5-7 \end{aligned}$ | R6 |
| P | D |  | 59056837723 | x | x |  |  |  |  | D | B119 | RESISTOR, FIXED, COMPOSITION: 81349: RC07GF1S2J | EA |  | 1 |  |  |  |  |  |  |  | 3 | $\begin{aligned} & -15 \\ & 5-7 \end{aligned}$ | R7 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (6) <br> QTY <br> INC <br> UNIT |  |  |  | (8) <br> 45 DAY AREA RESUPPLY ALLOW. BASED ON NO. EQUIP. SUPPORTED |  |  | $\begin{array}{\|c\|} \hline \text { (9) } \\ 1 \mathrm{YR} . \\ \text { ALW. } \\ \text { PER } \\ 100 \\ \text { EQUUP } \\ \text { CNTG } \\ \text { CY PL. } \\ \hline \end{array}$ | (10) <br> DEPOT <br> MAINT <br> ALW. <br> PRR <br> 100 <br> EQUIP. | $\stackrel{(11)}{ }_{\text {ILLUSTRATIONS }}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} \text { (A) } \\ \text { SRCE } \\ \text { CD } \end{gathered}$ | (B) <br> MNTC <br> DC | $\begin{array}{\|c\|c} \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | ${ }^{(2)}$ | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (A) | (B) |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ |  |  | (B) | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ |  |  |  | $\begin{aligned} & \text { (B) } \\ & 6-10 \end{aligned}$ |  | $\begin{array}{\|c\|c\|} \hline \text { (C) } 20 \end{array}$ |  | GN |
| P | D |  | 59058016444 | x | x |  |  |  |  | D | B161 | RESISTOR, FIXED, COMPOSITION: <br> 81349: RC07GF911J |  | EA |  | 5 |  |  |  |  |  |  |  |  | 15 | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R14 |
|  |  |  | 59058016444 | x | x |  |  |  |  | D | B162 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B161 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-8$ | R18 |
|  |  |  | 59058016444 | x | x |  |  |  |  | D | B163 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B161 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-8$ | R22 |
|  |  |  | 59058016444 | x | x |  |  |  |  | D | B164 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B161 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-8$ | R26 |
|  |  |  | 59058016444 | x | x |  |  |  |  | D | B165 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS 8161 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R30 |
| P | D |  | 59056870000 | x | x |  |  |  |  | D | B166 | RESISTOR, FIXED, COMPOSITION: 81349: RC07GF183J | EA |  | 5 |  |  |  |  |  |  |  | 15 | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R15 |
|  |  |  | 59056870000 | x | x |  |  |  |  | D | B167 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B166 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R19 |
|  |  |  | 59056870000 | X | x |  |  |  |  | D | B168 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B166 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R23 |
|  |  |  | 59056870000 | x | x |  |  |  |  | D | B169 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B166 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R27 |
|  |  |  | 59056870000 | x | x |  |  |  |  | D | B170 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B166 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R31 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (6) | $\qquad$ |  |  | (8)45 DAY AREARESUPPLY ALLOW.BASED ON NO.EQUIP. SUPPORTED |  |  | (9) <br> 1 YR. <br> ALW. <br> PER <br> 100 <br> EQUP <br> CNTG <br> CY PL. |  | $\stackrel{(11)}{\text { illustrations }}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (A) <br> SRCE <br> CD | (B) <br> MNTC DC | $\begin{array}{\|c\|} \hline \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ |  | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  | $\left\lvert\, \begin{gathered} \text { INC } \\ \text { IN } \\ \text { UNIT } \end{gathered}\right.$ |  |  |  | (A) FIGURE | (B) ITEM NO. |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ | $\begin{gathered} \left(\left.\begin{array}{c} 18 \\ 6-10 \end{array} \right\rvert\,\right. \end{gathered}$ | (C) (C) | $\begin{aligned} & \text { (A) } \\ & 1-5 \end{aligned}$ |  |  |  | $\begin{array}{\|c\|c\|} (\text { B }) \\ \text { (B) } \end{array}$ |  | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ |  | DESIGN |
| P | D |  | 59056832236 | X | X |  |  |  |  | D | B171 | RESISTOR, FIXED, COMPOSITION: <br> 81349: RC07GF391J |  | EA |  | 6 |  |  |  |  |  |  |  |  | 18 | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R16 |
|  |  |  | 59056832236 | x | x |  |  |  |  | D | B172 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B171 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R20 |
|  |  |  | 59056832236 | x | x |  |  |  |  | D | B173 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B171 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R24 |
|  |  |  | 59056832236 | x | x |  |  |  |  | D | B174 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B171 | EA |  | REF |  |  |  |  |  |  |  |  | -15 $5-8$ | R28 |
|  |  |  | 59056832236 | x | x |  |  |  |  | D | B175 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B171 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R32 |
|  |  |  | 59056832236 | x | x |  |  |  |  | D | B176 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS B171 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R41 |
| P | D |  | 59050518012 | X | X |  |  |  |  | D | B177 | RESISTOR, FIXED, FILM: 81349: RN60D7321F | EA |  | 1 |  |  |  |  |  |  |  | 3 | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R33 |
| P | D |  | 59056832246 | x | x |  |  |  |  | D | B178 | RESISTOR, FIXED, COMPOSITION: 81349: RC07GF473J | EA |  | 2 |  |  |  |  |  |  |  | 6 | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R34 |
|  |  |  | 59056832246 | x | x |  |  |  |  | D | B179 | RESISTOR, FIXED, COMPOSITION: <br> SAME AS 8178 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R39 |
| P | D |  | 59056824097 | x | x |  |  |  |  | D | B180 | RESISTOR, FIXED, COMPOSITION: <br> 81349: RC07GF302J | EA |  | 1 |  |  |  |  |  |  |  | 3 | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | R35 |

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| (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (6) <br> QTY <br> INC <br> $\underset{\text { UNIT }}{\text { IN }}$ |  |  |  | (8) <br> 45 DAY AREA <br> RESUPPLY ALLOW. <br> BASED ON NO. <br> EQUIP. SUPPORTED |  |  | (9) <br> 1 YR. <br> ALW. <br> PER <br> 100 <br> EQUP <br> CNTG <br> CY PL. | (10)DEPOTMAINTALW.PER100EQUIP. | $\stackrel{(11)}{\text { illustrations }}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} \text { (A) } \\ \text { SRCE } \\ \text { CD } \end{gathered}$ | (B) <br> Mntc DC | $\begin{array}{\|c\|} \hline \text { (C) } \\ \text { REC } \\ \text { CODE } \end{array}$ | ${ }_{\text {FEDERAL }}^{(2)}$ | REPAIR PARTS FOR ON-SITE, AREA RESUPPLY, AND DEPOT MAINTENANCE |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\stackrel{\text { (A) }}{\text { Figure }}$ | (B) ITEM NO. |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & (\mathrm{A}) \\ & 1-5 \end{aligned}$ |  |  | $\begin{gathered} (\mathrm{B}) \\ 6-10 \end{gathered}$ | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ | $\begin{gathered} \text { (A) } \\ 1-5 \\ \hline \end{gathered}$ |  |  |  | $\begin{array}{\|c\|c\|} \hline \text { (B) } \\ \hline \text { (B) } \end{array}$ |  | $\begin{gathered} \text { (C) } \\ 11-20 \end{gathered}$ |  | DESIGN |
| P | D |  | 59619952310 | X | x |  |  |  |  | D | B191 | SEMI-CONDUCTOR DEVICE DIODE 81349: JAN1N752A |  | EA |  | 5 |  |  |  |  |  |  |  |  | 15 | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | VR1 |
|  |  |  | 59619952310 | x | x |  |  |  |  | D | B192 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B191 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | VR2 |
|  |  |  | 59619952310 | x | x |  |  |  |  | D | B193 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B191 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | VR3 |
|  |  |  | 59619952310 | x | x |  |  |  |  | D | B194 | SEMI-CONDUCTOR DEVICE, DIODE: SAME AS B191 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | VR4 |
|  |  |  | 59619952310 | x | x |  |  |  |  | D | B195 | SEMI-CONDUCTOR DEVICE DIODE: SAME AS B191 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | VR5 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B196 | TRANSISTOR: SAME AS B065 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | Q1 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B197 | TRANSISTOR: SAME AS B065 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | Q2 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B198 | TRANSISTOR: <br> SAME AS B055 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | Q3 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B199 | TRANSISTOR: SAME AS B065 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | Q4 |
|  |  |  | 59610507499 | x | x |  |  |  |  | D | B200 | TRANSISTOR: <br> SAME AS B065 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | Q5 |
|  |  |  | 59610507499 |  | x |  |  |  |  | D | B201 | TRANSISTOR: <br> SAME AS B065 | EA |  | REF |  |  |  |  |  |  |  |  | $\begin{aligned} & -15 \\ & 5-8 \end{aligned}$ | Q6 |

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By Order of the Secretaries of the Army and the Navy:

Official:
W. C. WESTMORELAND, General, United States Army, Chief of Staff.

KENNETH G. WICKHAM, Major General, United States Army, The Adjutant General.

JOSEPH E. RICE,
Rear Admiral, U. S. Navy, Commander, Naval Electronics Systems Command.


Figure 3-1. Punched tape reader, block diagram.


Figure 3-19. Rectifier and regulator circuits, block diagram.


Figure 3-20. Power sequencing circuits, block diagram.


| Identification label <br> High woltage warning label Screw, panhead, $6-32,5 / 26$ in. long <br> lockwasher, internal tooth, No. 6 <br> Hex nut, Keps, 6-32 <br> Screw, pauhead, 6-32,3/4 in. long Washer, plain, No. 6 Clamp bar <br> Capstan drive guard <br> screw, flathead, 6-32, 1/2 in. long, Nyiloc Fan guard <br> Screw, panhead, $4-40,3 / 8 \mathrm{in}$. long Washer, plain, No. 4 Bottom cover <br> Screw, sockethead, 4-40, 5/16 in. long Wazher, plain, No. 4 <br> Rearing plate <br> Grip ring <br> Roler assembly <br> Grip ring <br> Holler asembly <br> Support pin <br> Setscrew, iocke., 6-32, $1 / 4$ in. Long Roller support shaft Roller support 23.1 Roller support Spring retainer <br> Tight tape spring <br> Setsicrew, soeket, $2-56,1 / 8 \mathrm{in}$. long <br> Setserew, socket, 6-32,3/16 in. long <br> Lockwasher, split, No. 6 Screw, roundhead, $\mathrm{fi} 32,3 / 16 \mathrm{in}$. long <br> Stop Screw, flachea: 6-32, 5/8 in. hong <br> Hex nut, Keps, 6-?2 <br> Screw, panhead, 2-56, $3 / 8 \mathrm{in}$. long <br> Washer, plain. No. 2 Lockwasher, internal twoth, No. 2 <br> Actuator <br> Switch 40.1 Tight tape cable <br> Frame assembly <br> Screw, panhead, 4-40, $3 / 8 \mathrm{in}$. long <br> Washer, split-ring, No Washer, piain, No. 4 <br> Cower cover bracket <br> Screw, flathead, 4-40, 5/16 in. long Drive belt <br> Screw, cup pt., $4-401 / 4 \mathrm{in}$. long 1d-tooth paliey Capstan <br> Capsta <br> Screw, socicethead, 8-32, 3/8 2... long <br> Read head and track assernbly <br> Cam <br> Setscrew, socket, 6-32, 3/16 in, long <br> Not used Slew lever |  |  |
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. Panel bubhang
















 nesed . Janneifor block brackekt







Figure 4-12. Reader mechanism A2, exploded view.


Figure 8-1. Punched tape reader, interconnection schematic diagram. (Part 2 of 2)


Figure 8-1.1. Transmission identification generator, interconnection schematic diagram.


[^4]Figure 8-2. Punched tape reader control panel, schematic diagram.


Figure 8-3. Ac and dc circuits, schematic diagrams (part 1 of 2).

## Change 2 8-7



Figure 8-3. Ac and dc circuits, schematic diagrams (part 2 of 2).


Figure 8-3.1 Ac and dc circuits, schematic diagrams (part 1 of 2). (with TIG installed)

Change 6 8-10.1/(8-10.2 blank)


Figure 8-3.1 Ac and dc circuits, schematic diagrams (part 2 of 2).
(with TIG installed)


Figure 8-4. (1). Rectifier and regulator circuits, schematic diagram (part 1 of 3)


Figure 8-4 (2). Rectifier and regulator circuits, schematic diagram (part 2 of 3).


Figure 8-4 (3). Rectifier and regulator circuits, schematic diagram (part 3 of 3).

Change 2 8-15


1 Figure 8-5. Power sequencing circuits, (PS1A12), schematic diagram.


Figure 8-6 (1). Reader mechanism assembly A2, schematic diagram (part 1 of 2).

## NOTES:

 2. UNEESS OTHERWISE SPECFIED:


| Powfa ineut pins |
| :--- | :--- | :--- |
| T | |  | $21,22,23$ |
| :---: | :---: |
| +4 sNoC | 6 |
| Gro | 1 |



FOR PUNCHED TAPE UNITS HAVING TIG ASSEMBLY A7 OR A8 INSTALLED, REFER TO FIGURE 8-23.1.

Figure 8-7. PC card A1 (No. A65209-001), schematic diagram.

NOTES:

2. WLESS OTEFWISE SPECFIFE:

| powe ineur PMS |  |
| :---: | :---: | :---: |
|  | $21,22,23$ |
| +4 Sid | 6 |




(TB2-4B)



Figure 8-7.1. PC card A1 (No. A65209-001), schematic diagram. (with TIG installed)

Change 8 8-24.1


NOTE:
partial reference designations are shown FOR COMPLETE DESIGNATION PREFIX WITH UN FOR COMPLE TE DESIGNATION PREFIXION (S)

| POWER INPUT PINS |  |
| :---: | :---: |
|  | $Z 1$ THRU 25 |
| +12 VDC | 7 |
| $-12 \mathrm{~V} D C$ | 8 |
| GRD | 10 |
| LAMP TEST | 9 |



## NOTES:

1. partila reference designations are shown; for complete PARTILL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLET
DESNATON PREFIX WITH UNIT NUMBER OR SUBASSEMBLY

2. UNLESS OTHERWISE SPECIFIED
all resistance values are in ohms.



FOR PUNCHED TaPE READERS HAVING TIG ASSEMBLY a7 or a 8 INSTALLED, REFER TO FIGJRE 8-10.3.

Figure 8-10. PC card A5 (No. A65205-001), schematic diagram.
Change 4 8-29/(8-30 blank)


Figure 8-10.3. PC card A5 (No. A65205-001), schematic diagram. (with TIG installed)


NOTE


TM7440-219-15-60-1

Figure 8-11. PC card A6 (No. A65421-001), schematic diagram


Figure 8-11.1. PC card A6 (No. A665421-001), schematic diagram. (with TIG installed)








NOTES:

1. PARTTAL REEERENCE DESIGNATIONS ARE SHOWN:
2.UNLESS OTHERWISE SPECLIF

FOR PUNCHED TAPE READERS HAVING TIG ASSEMBLY FOR OR 48 INSTALLED, REFER TO FIGURE 8-12.1.

Figure 8-12. PC card A7 (No. A65426-001), schematic diagram.

(xAS-C) +2voct




NOTES:



Figure 8-12.1. PC card A7 (No. A65426-001), schematic diagram

note:


$414040-210-18-70$

Figure 8-13. PC and A8 (No. A63418-001), schematic diagram.


Figure 8-14. PC card A9 (No. A53725-001), schematic diagram.


Figure 8-15. PC card A10 (No. A53721-001), schematic diagram.


Figure 8-16. PC card A11 (No. A53725-001), schematic diagram.


Figure 8-17. PC card A12 (No. A53721-001), schematic diagram.


Figure 8-18. PC card A13 (No. A53434-001), schematic diagram.
Change 4 8-45
(8-46 blank)


NOTES:
 FOR PUNCHED TAPE READERS HAVING TIG ASSEMBLY
H7 OR A8 INSTHLLED, REFER TO FIGURE $8=19.1$



Figure 8-19. PC card A14 (No. A65433-001), schematic diagram.

notes:




Figure 8-19.1. PC card A14 (No. A65433.001). schematic diagram .
(with TIG installed)
Change 8 8-48.1


NOTES:




FOR PUNCHED TAPE READERS HAVING TIG ASSEMBLY
A7 OR A8 INSTALLED, REFER TO FIGURE $8-20.1$.


Figure 8-20. PC card A16 (No. A65437-001), schematic diagram.
Change 4 8-49
(8.50 blank)


NOTES:

| power infut pins |  |
| :---: | :---: |
|  | 22 TMRU 224,726.727.228 |
| +4.svoc | 6 |
| GRD | 1 |




notes:




FOR PUNCHED TAPE READERS HAVING THG ASSEMBLY
AT OR AB INSTALIED, SEE FIGURE 8 ILI.

Figure 8-21. PC card A16 (No. A65429-001), schematic diagram.



Figure 8-21.1. PC card A16 (No. A65429-001), schematic diagram. (with TIG installed)

Change 4 8-52.1
(8-52.2 blank)


Figure 8-21.2. PC card A2 (NO. 12 -890081), schematic diagram.

## Change 6 8-52.3/ (8-52.4 blank)



Figure 8-21.3. PC card A7A1 (NO. 12 -890082), schematic diagram.


Figure 8-22. Military standard for color code marking.
Change 7 8-53/(8-54 blank)
All data on pages $8-55$ and $8-56$, including figure 8 - 23 deleted.



[^0]:    ${ }^{\text {a }}$ Used on dual punched tape reader unit.
    ${ }^{\mathrm{b}}$ Used on single punched tape reader unit.

[^1]:    1 Screw, panhead 6-32, 3/8 in. Long
    Lockwasher, No. 6
    Washer, flat, No. 6
    Tape guide

[^2]:    1 Hex nut, No. 4-40
    2 Lockwasher, No. 4
    3 Washer, No. 4

[^3]:    Change 6 D-7

[^4]:    NOTE:

